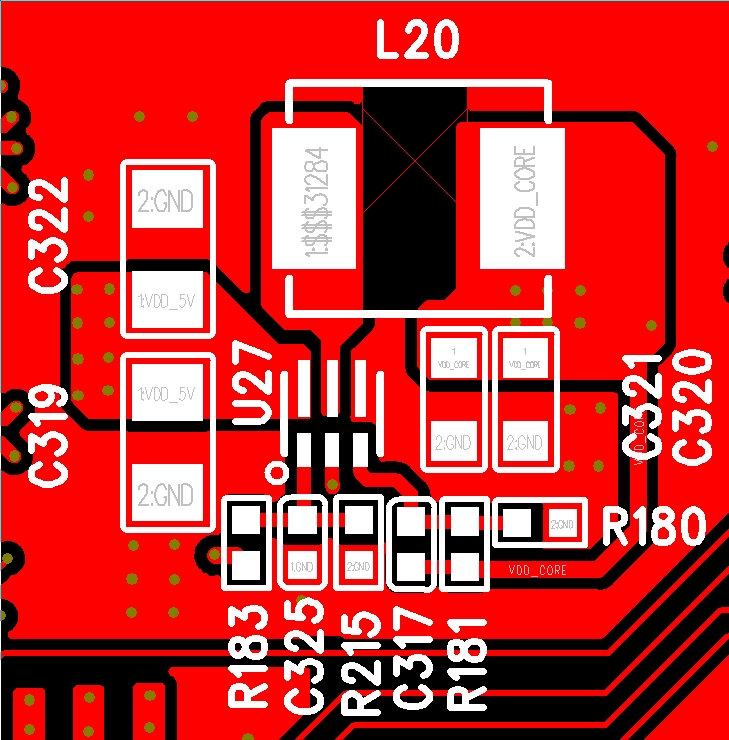
Update 2023-03-27

The PCB layers are routed as follows:

DC-DC cabling is on the top floor and 8th floor. The inner sub-top floor and sub-low floor are the ground reference. There are two power layers and two cabling layers in the middle.

1. TOP

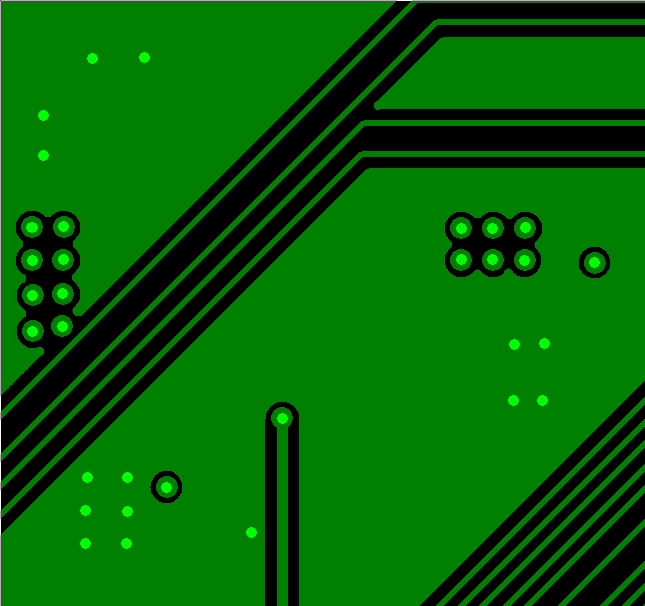


1. GND

图片包含 示意图

描述已自动生成

1. L3



1. POWER1

图表, 散点图

描述已自动生成

1. Power2

图片包含 图示

描述已自动生成

1. L6

图片包含 游戏机, 电子, 电路

描述已自动生成

1. GND2

图片包含 图示

描述已自动生成

1. BOT

图示

描述已自动生成

2023-03-23

1. The existing product board uses TLV62595DMQR 5.0V input and 0.92V output to provide our CPU with core voltage and current 2.4A. The schematic diagram is as follows：

图示

描述已自动生成

1. In the process of signal testing, it was found that SW signal jitter and oscilloscope could not trigger, as shown in the first figure ， stop oscilloscope, locally amplify the signal, ringing occurs. The second figure ：

电脑萤幕画面

中度可信度描述已自动生成

（1）

图示

描述已自动生成

（2）

1. On the same product module, run the TLV62569DBV 5V to 1.2V for DDR4. No jitter is detected, but ringing occurs.

电脑萤幕画面

中度可信度描述已自动生成

The customer has compared the schematic diagram of TLV62595DMQREVM board and found no significant difference.

How to solve the jitter and ringing problems? There is no relevant TI application document available？