Update 2023-04-06

1. The experiment of adding a capacitor between input Vin and GND in the nearest distance of TLV62595DMQR. Due to space limitation and the constricting condition of VSON-HR package pins, the customer cannot conduct this experiment welding.

If there is PCB change board, the customer will follow your instructions.

1. 0.9V capacitance in other pages see figure below

图示

描述已自动生成

1. The input of TPS62827EVM-036 EVM board is connected to 5V of the customer's product board, and the output is connected to Vcore 0.9V (the original 0.9V inductance on the board is removed by welding). At this time, the jitter of TLV62595DMQR on the original board will be reduced. The ripple will change from 60mV to 40mV, decreasing by 20mV.

电脑萤幕画面

中度可信度描述已自动生成

图形用户界面

描述已自动生成

Update 2023-03-31

The customer does not have TLV62595DMQR EVM,but has TPS62827 EVM. The two chips are pin to pin compatible.

图片包含 图示

描述已自动生成

Use an external power supply to input 5V to the EVM, output 0.92V, add different metal shell resistance load, make the output current up to 1A, 3.2A.

The SW signal under two kinds of current load was measured respectively, and there was smaller jitter compared with our product board.

This test method only involves resistance, almost does not consider the inductive and capacitive load.

图示

中度可信度描述已自动生成

电视游戏的萤幕截图

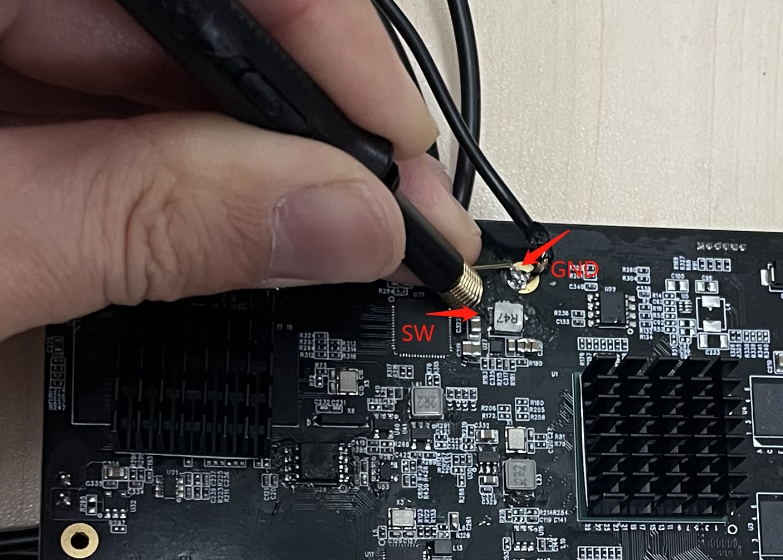
描述已自动生成

In order to eliminate the problem of oscilloscope and measurement method, the customer measured the SW signal of TLV62569DBV on the product board at the same time, 5V to 3.3V,1A load. The jitter was significantly smaller, which could be almost ignored by the naked eye, as shown in the figure below:



Update 2023-03-28

1. The test method and device are shown below. In order to reduce the loop area and avoid coupling interference, the oscilloscope probe uses a ground spring.



1. The oscilloscope is Rigal MSO2302A 300Mhz bandwidth, 2GSa/s sampling rate.

图形用户界面, 应用程序

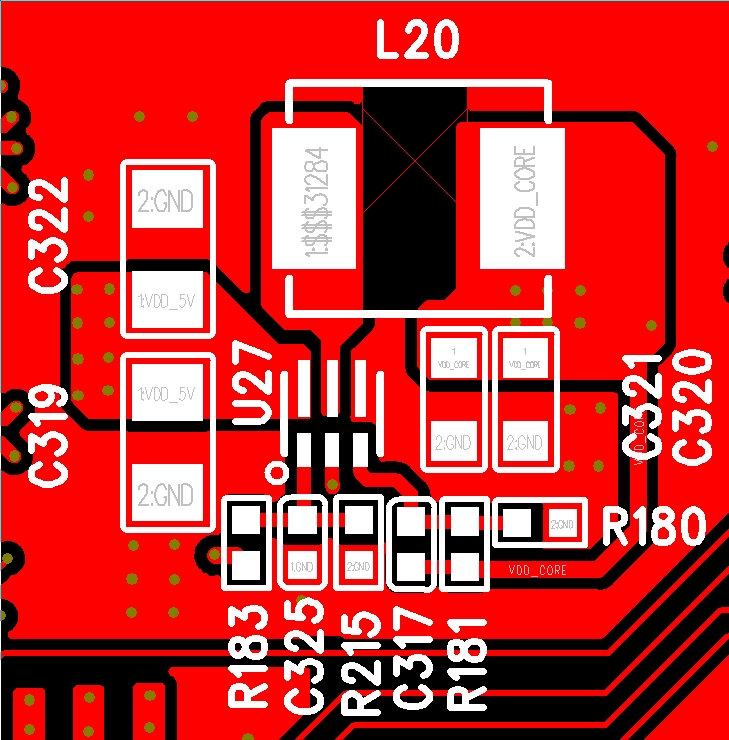
描述已自动生成

Update 2023-03-27

The PCB layers are routed as follows:

DC-DC cabling is on the top floor and 8th floor. The inner sub-top floor and sub-low floor are the ground reference. There are two power layers and two cabling layers in the middle.

1. TOP

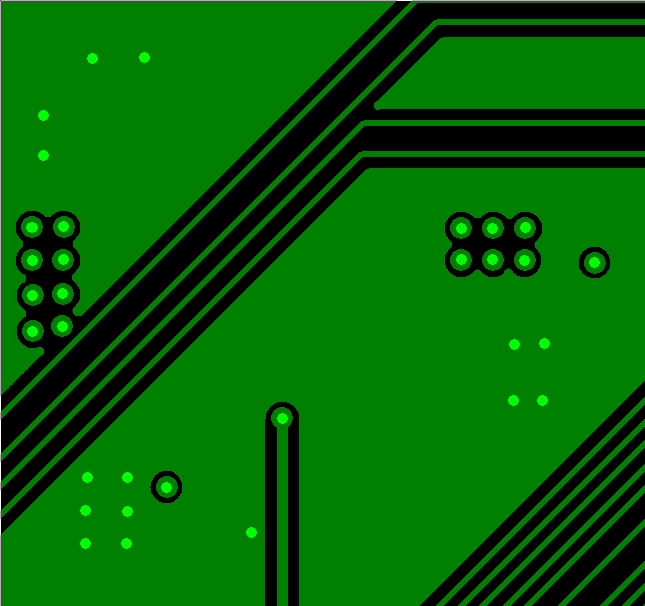


1. GND

图片包含 示意图

描述已自动生成

1. L3



1. POWER1

图表, 散点图

描述已自动生成

1. Power2

图片包含 图示

描述已自动生成

1. L6

图片包含 游戏机, 电子, 电路

描述已自动生成

1. GND2

图片包含 图示

描述已自动生成

1. BOT

图示

描述已自动生成

2023-03-23

1. The existing product board uses TLV62595DMQR 5.0V input and 0.92V output to provide our CPU with core voltage and current 2.4A. The schematic diagram is as follows：

图示

描述已自动生成

1. In the process of signal testing, it was found that SW signal jitter and oscilloscope could not trigger, as shown in the first figure ， stop oscilloscope, locally amplify the signal, ringing occurs. The second figure ：

电脑萤幕画面

中度可信度描述已自动生成

（1）

图示

描述已自动生成

（2）

1. On the same product module, run the TLV62569DBV 5V to 1.2V for DDR4. No jitter is detected, but ringing occurs.

电脑萤幕画面

中度可信度描述已自动生成

The customer has compared the schematic diagram of TLV62595DMQREVM board and found no significant difference.

How to solve the jitter and ringing problems? There is no relevant TI application document available？