

TPS65941213-Q1 and TPS65941111-Q1 troubleshoot

Reference:

Optimized TPS65941213-Q1 and TPS65941111-Q1 PMIC User Guide for Jacinto 7 J721E, PDN-0C

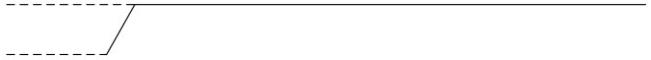
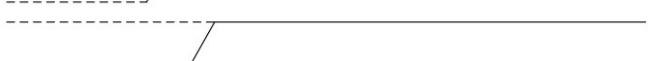
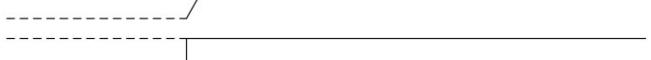
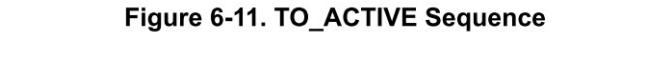
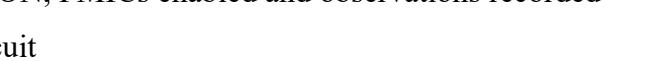
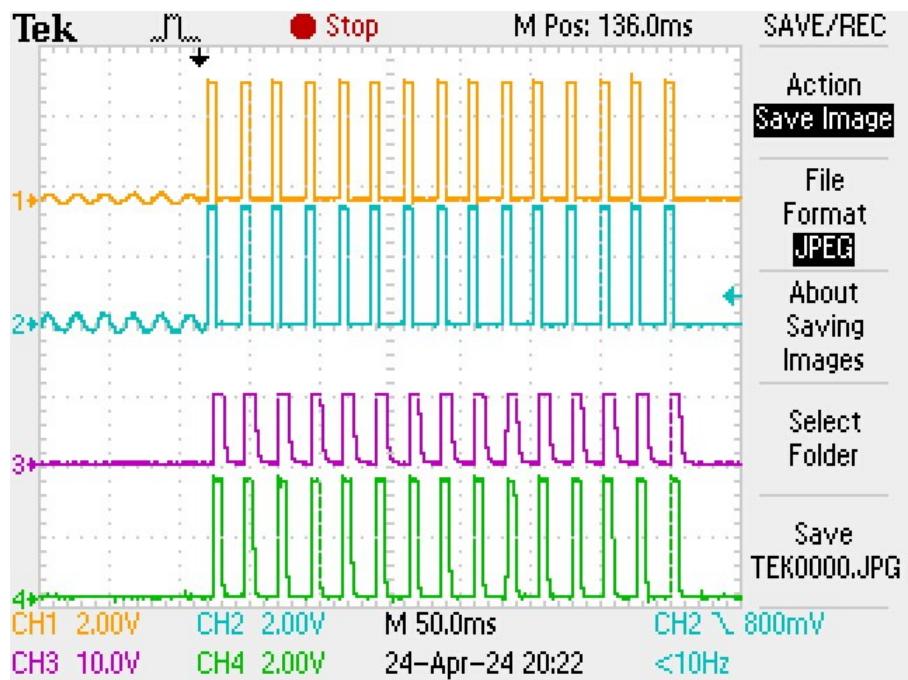
Resource	PMIC	Delay Diagram	Total Delay	Rail Name
GPIO9	TPS65941213-Q1		0 us	EN_MCU3V3IO_LDSW
GPIO11	TPS65941111-Q1		0 us	EN_3V3IO_LDSW
LDO2	TPS65941111-Q1		0 us	VDD_USB_3V3
LDO1	TPS65941111-Q1		0 us	VDD_SD_DV
LDO1	TPS65941213-Q1		1700 us	VDD1_DDR_1V8
LDO4	TPS65941213-Q1		1700 us	VDA MCU 1V8
BUCK5	TPS65941213-Q1		1700 us	VDD_PHY_1V8
LDO4	TPS65941111-Q1		1700 us	VDA_PLL_1V8
BUCK123	TPS65941213-Q1		2700 us	VDD_CPU(AVS)
LDO3	TPS65941213-Q1		2700 us	VDD_DLL_0V8
BUCK124	TPS65941111-Q1		2700 us	VDD_CORE_0V8
BUCK3 Monitor	TPS65941213-Q1		3700 us	mVDD MCUIO_3V3
BUCK4	TPS65941213-Q1		3700 us	VDD MCU 0V85
LDO2	TPS65941213-Q1		3700 us	VDD MCUIO 1V8
BUCK5	TPS65941111-Q1		3700 us	VDD RAM 0V85
LDO3	TPS65941111-Q1		3700 us	VDD IO 1V8
GPIO3	TPS65941111-Q1		3700 us	EN_VDDR
nRSTOUT	TPS65941213-Q1		12700 us	H MCU PORz 1V8
nRSTOUT_SOC	TPS65941213-Q1		12700 us	H SOC PORz 1V8

Figure 6-11. TO_ACTIVE Sequence

Test Setup:

- 1) The card is powered ON, PMICs enabled and observations recorded
- 2) No change in the circuit

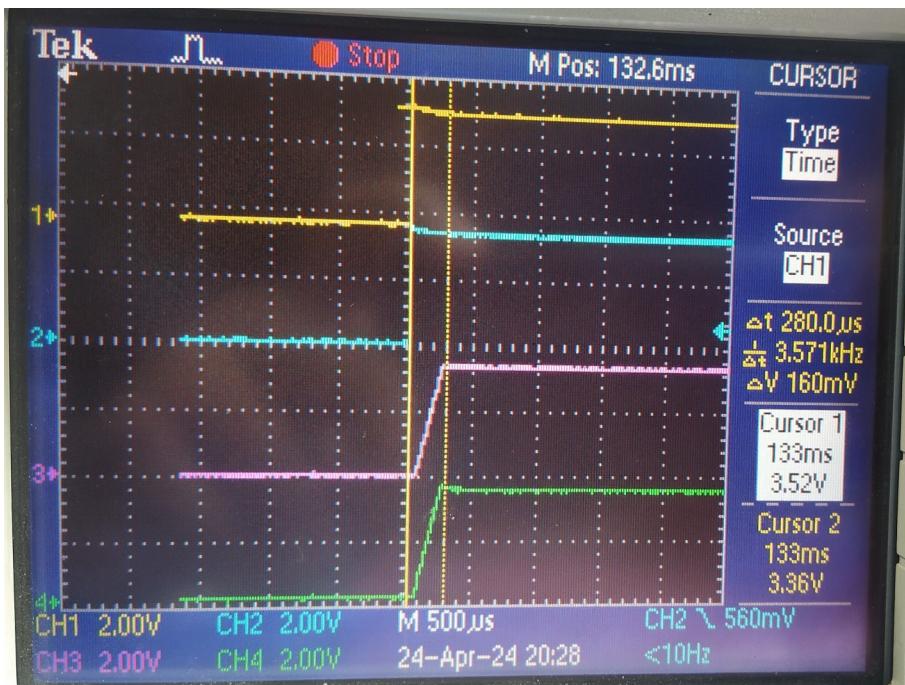
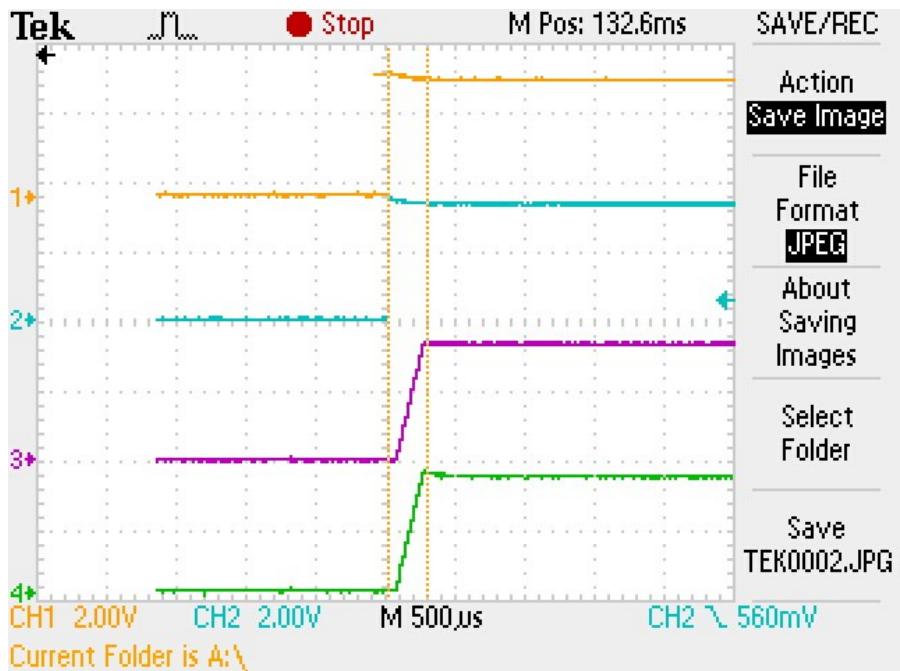
GPIO-9 retries



Signal 1 : GPIO-9 of TPS65941213-Q1

15 retries can be observed here

GPIO-9 and GPIO-11, LDO2, LDO1



Signal1: GPIO-9 of TPS65941213-Q1

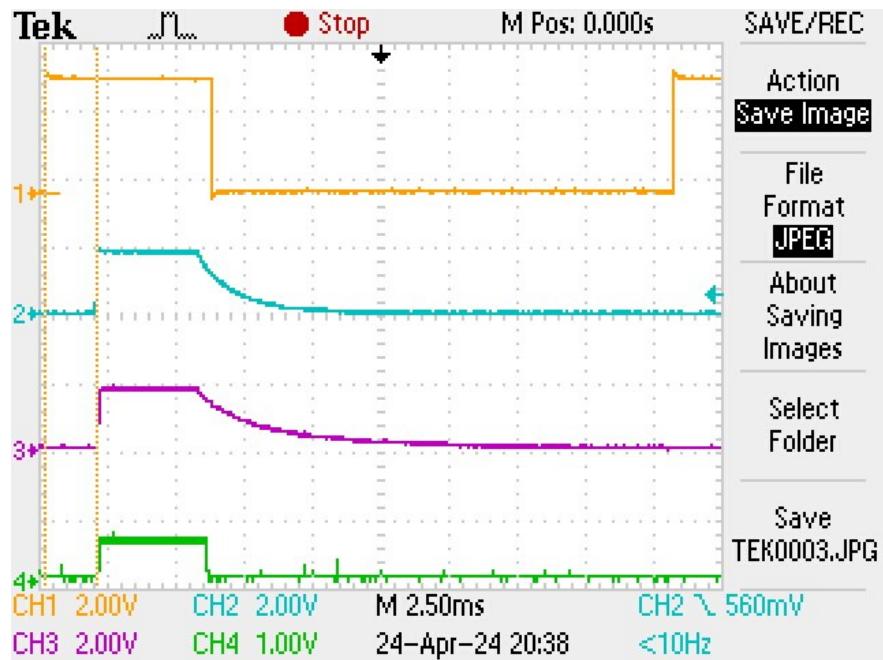
Signal 2: GPIO-11 of TPS65941111-Q1

Signal 3: LDO2 of TPS65941111-Q1

Signal 4: LDO1 of TPS65941111-Q1

All the signals start to rise at the same instant, in agreement with the TO_ACTIVE FSM

GPIO-9 and LDO1, LDO4, BUCK5



Signal1: GPIO-9 of TPS65941213-Q1

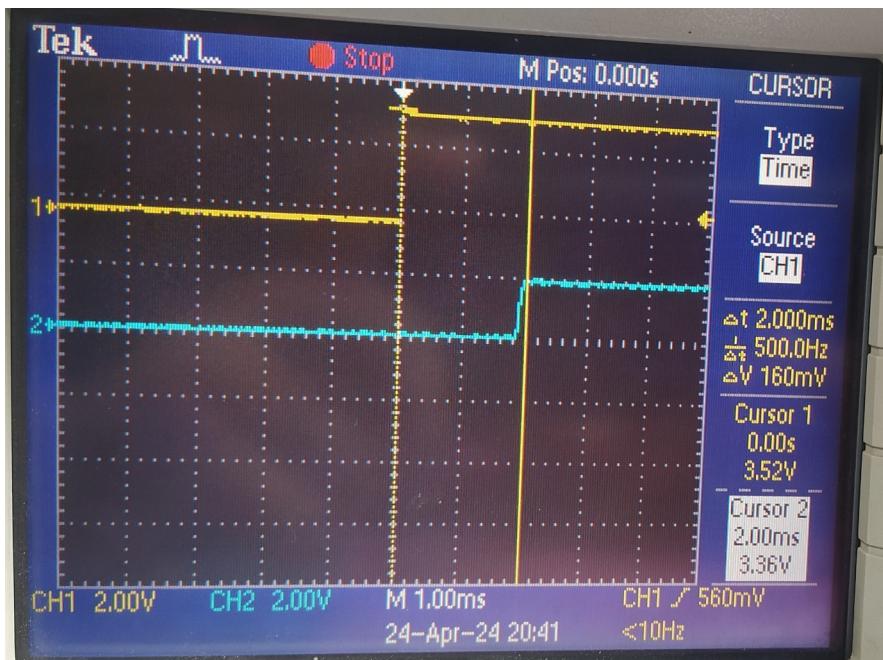
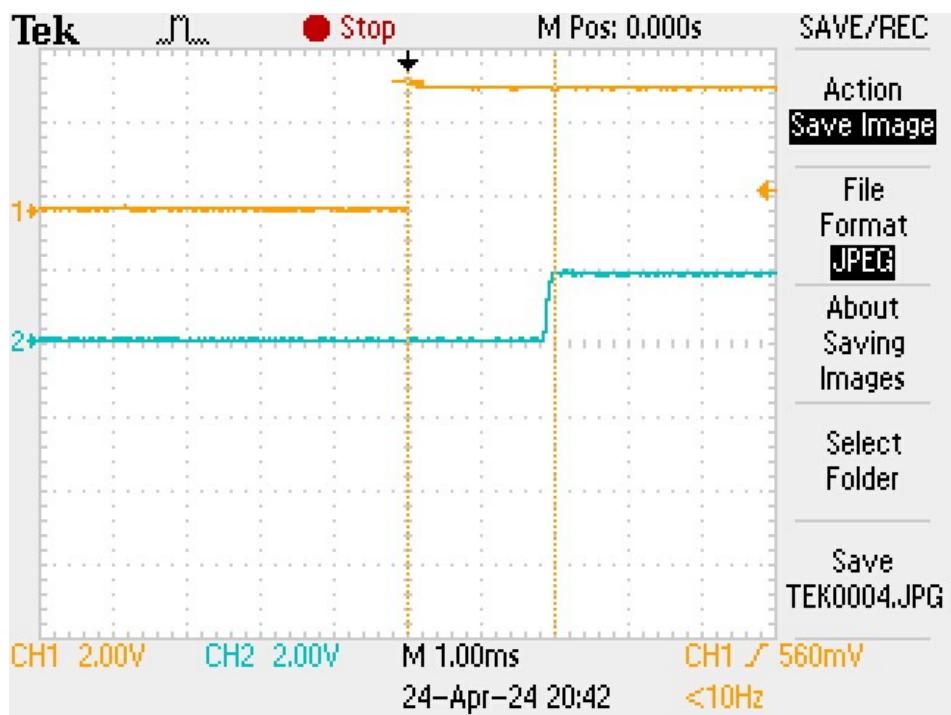
Signal 2: LDO1 of TPS65941213-Q1

Signal 3: LDO4 of TPS65941213-Q1

Signal 4: BUCK5 of TPS65941213-Q1

Signals 2,3, and 4 begin to rise at approx 1900us after GPIO-9 in agreement with the TO_ACTIVE FSM (1700us is mentioned in the application notes)

GPIO-9 and LDO1



Signal1: GPIO-9 of TPS65941213-Q1

Signal 2: LDO4 of TPS65941111-Q1

Signal 2 begins to rise at approx 1900us after GPIO-9 in agreement with the TO_ACTIVE FSM
(1700us is mentioned in the application notes)

Note: Following LDO4, the other signals in the sequence are at 0V