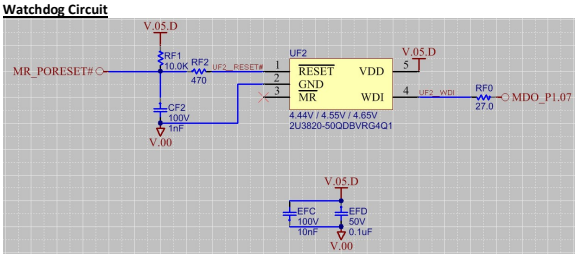
Cold Boot Issue with TPS3820 Voltage Monitor

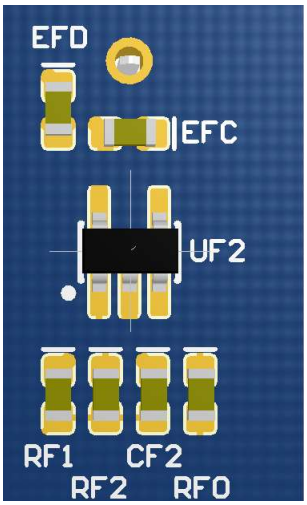
Monday, December 17, 2018 1:48 PM

Background

1. We have used the TI TPS382 voltage monitor with watchdog timer successfully on a number of automotive embedded 8-bit controllers (MCU) since 2009 (5 volts).
   a. The original part # was: 2U3820-50QDBVRG4Q1
   b. The new AEC-Q100 # is: TPS3820-50QDBVRQ1
2. On a recent project, cold weather testing at 5'C has revealed that 8 out of 16 MCUs don't immediately come out of reset. Once the boards warm up from 30s to 90s, the reset line de-asserts and the MCU run normally. No power cycle is involved to get reset to de-assert.
3. The contention repeats 100% on all boards if soaked at -18'C for 1 hour.
4. The original part has been used for several years and does not experience the cold issue.
   a. However, there has been an update to the Iso DC/DC power supply.

Watchdog Circuit





Experimental Setup

The above circuitry was instrumented using a Saleae Logic Pro 16 dual logic analyzer / analog scope.
The following signals were sampled at 125MHz digital and 3.125Mhz analog.

1. V.05.D
   a. Digital 5V supply rail measured at jtag header 5.5mm from UF2
2. PORESET#
   a. Global power on reset measured at jtag header
   b. Connects XC878 8-bit micro and Si8652BC-B-IS1 SciLab digital isolator enable line
3. UF2.RESET
   a. Measured directly on TPS3820 pin
4. UF2.WDI
   a. Measured directly on TPS3820 pin

The following table compares voltage readings for 3 experiments.
The "Pass" experiment illustrates a nominal boot at room temperature.
The "Fail" experiment uses the same board soaked for 1hr at -18'C.
The "Exp1 Pass" experiment changed RF0 from 27 to 1K (WDI series resistor).
All experiments have been repeated several times and are consistent.

All recordings show similar voltage readings and behavior.
Also if the TPS3820 is disconnected by removing RF2, the XC878 boots properly under all conditions .

Table 1, Voltage Readings

		Pass	Fail	Exp1 Pass
First Spike		0.11ms	0.13ms	0.13ms
	V.05D	0.75V	0.78V	0.77V
	PORESET#	0.76V	0.80V	0.78V
	UF2.RESET	0.62V	0.67V	0.66V
	UF2.WDI	0.11V	0.15V	0.21V
V.05D Stable		0.63ms	0.57ms	0.62ms
	V.05D	4.89V	4.88V	4.88V
	PORESET#	0.67V	0.66V	0.42V
	UF2.RESET	0.05V	0.05V	0.05V
	UF2.WDI	1.90V	2.11V	2.05V

Nominal Boot Sequence (Figures 1, 2 and 3)

1. At 0.1091ms from power-on, a first spike can be seen in all signals (Figures 1, 2 and 3)
   a. V.05.D: 0.75V
   b. PORESET#: 0.76V

c. UF2.RESET: 0.62V
d. UF2.WDI: 0.11V

2. At 0.625ms from power-on, V.05D stabilizes, RESET asserts low
   a. V.05.D: 4.89V
   b. PORESET#: 0.67V
   c. UF2.RESET: 0.05V
   d. UF2.WDI: 1.90V
3. At 29.83ms from power-on, RESET asserts high
   a. V.05.D: 4.98V
   b. PORESET#: 5.07V
   c. UF2.RESET: 4.98V
   d. UF2.WDI: 1.95V
4. At 49.34ms from power-on, WDI switches high signaling bootloader watchdog kicks
   a. UF2.WDI: 4.66V
5. At 280ms from power on, WDI switches according to application normal watchdog kicks

Failed Boot Sequence (Figures 4, 5 and 6)

1. At 0.1254ms from start, a first spike can be seen in (Figures 4, 5 and 6)
   a. V.05.D: 0.78V
   b. PORESET#: 0.80V
   c. UF2.RESET: 0.67V
   d. UF2.WDI: 0.15V
2. At 0.57ms, V.05d stabilized
   a. V.05.D: 4.88V
   b. PORESET#: 0.66V
   c. UF2.RESET: 0.05V
   d. UF2.WDI: 2.11V

Experiment 1 RF0 = 1K

1. Proper boot is achieved cold start with RF0 = 1K

Figure 1 Nominal Boot Warm

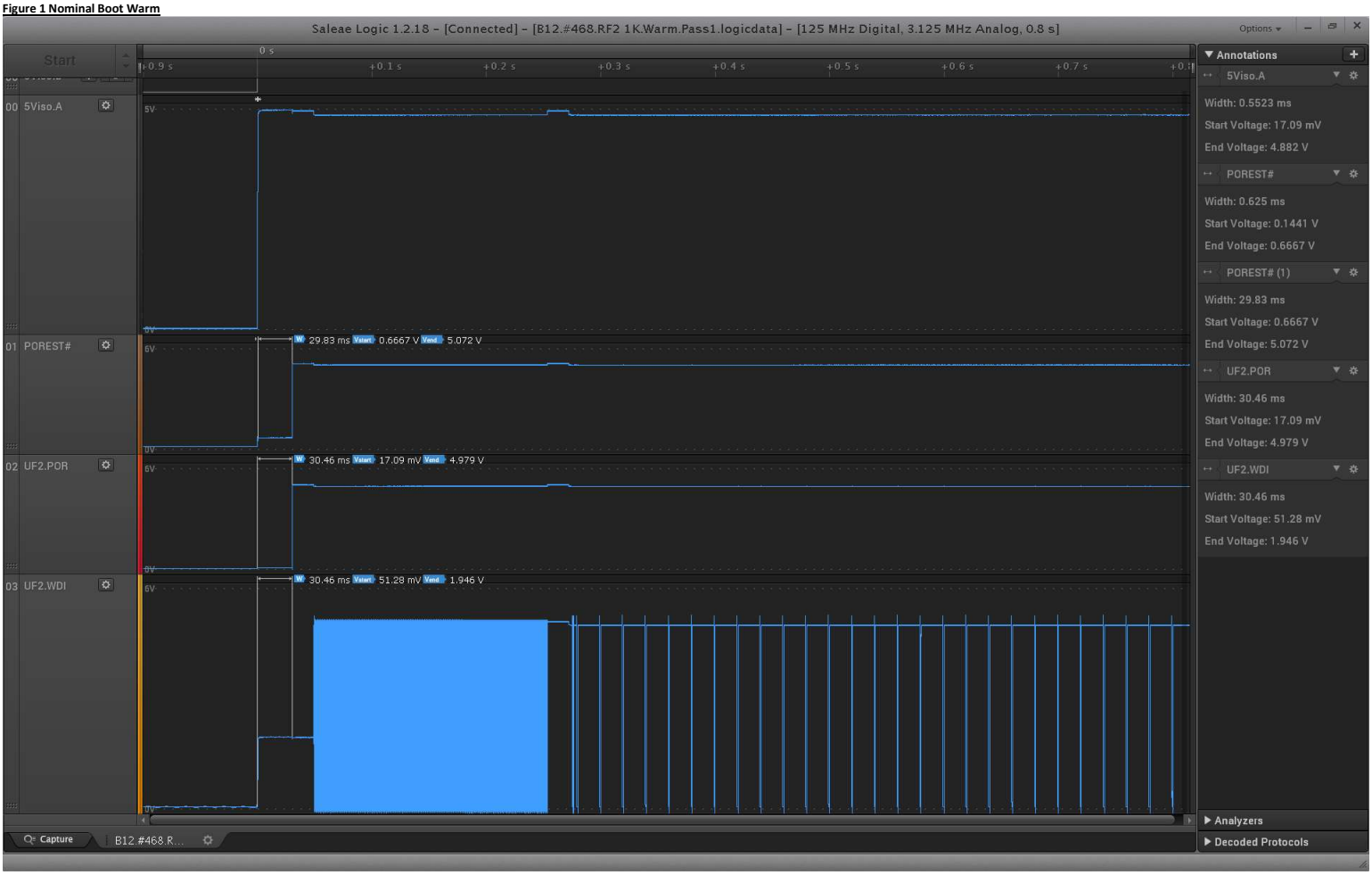


Figure 2 Nominal Boot Warm Zoom

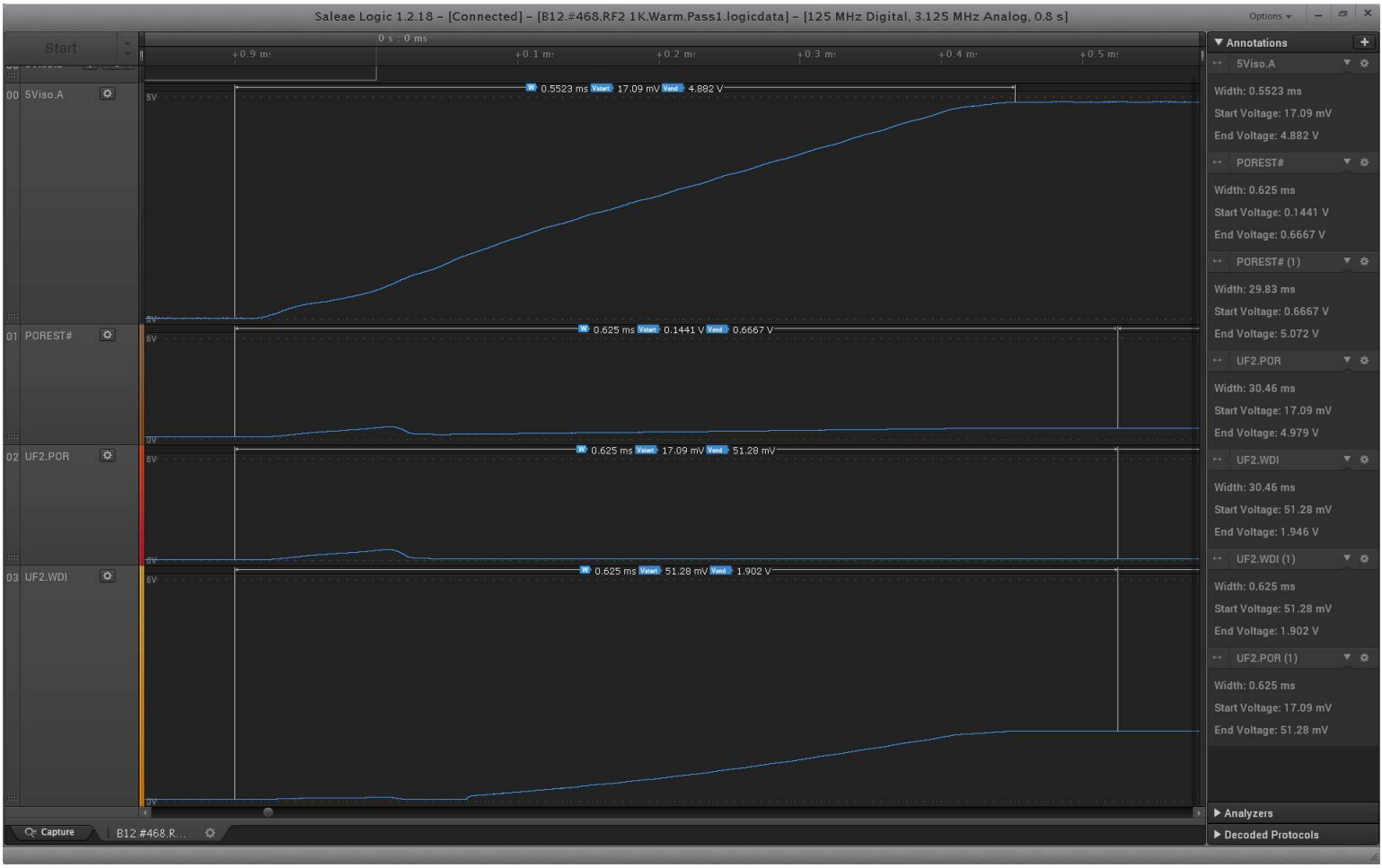


Figure 3 Failed Boot Cold

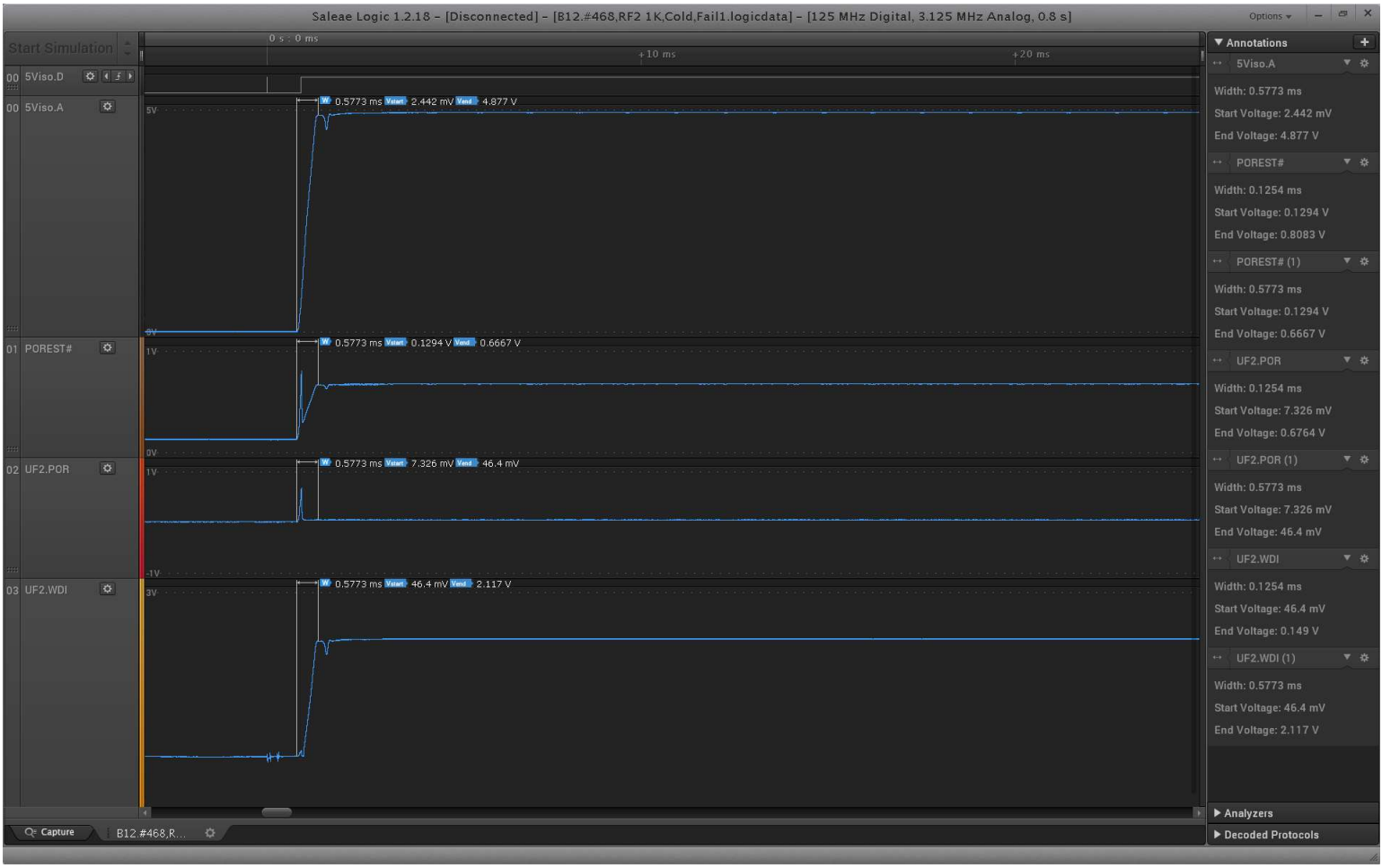


Figure 4 Failed Boot Cold Zoom 1

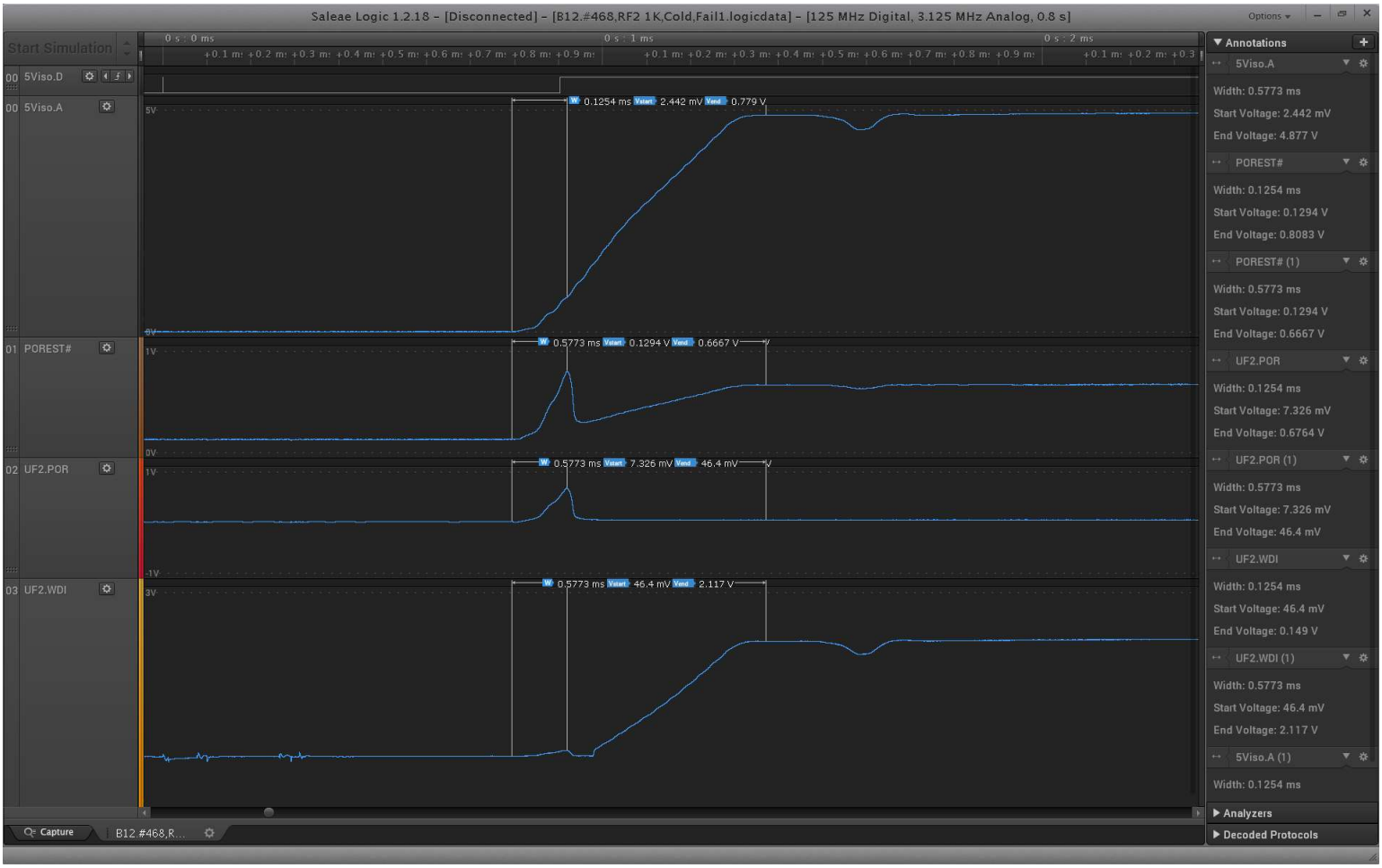


Figure 5 Failed Boot Cold Zoom 2

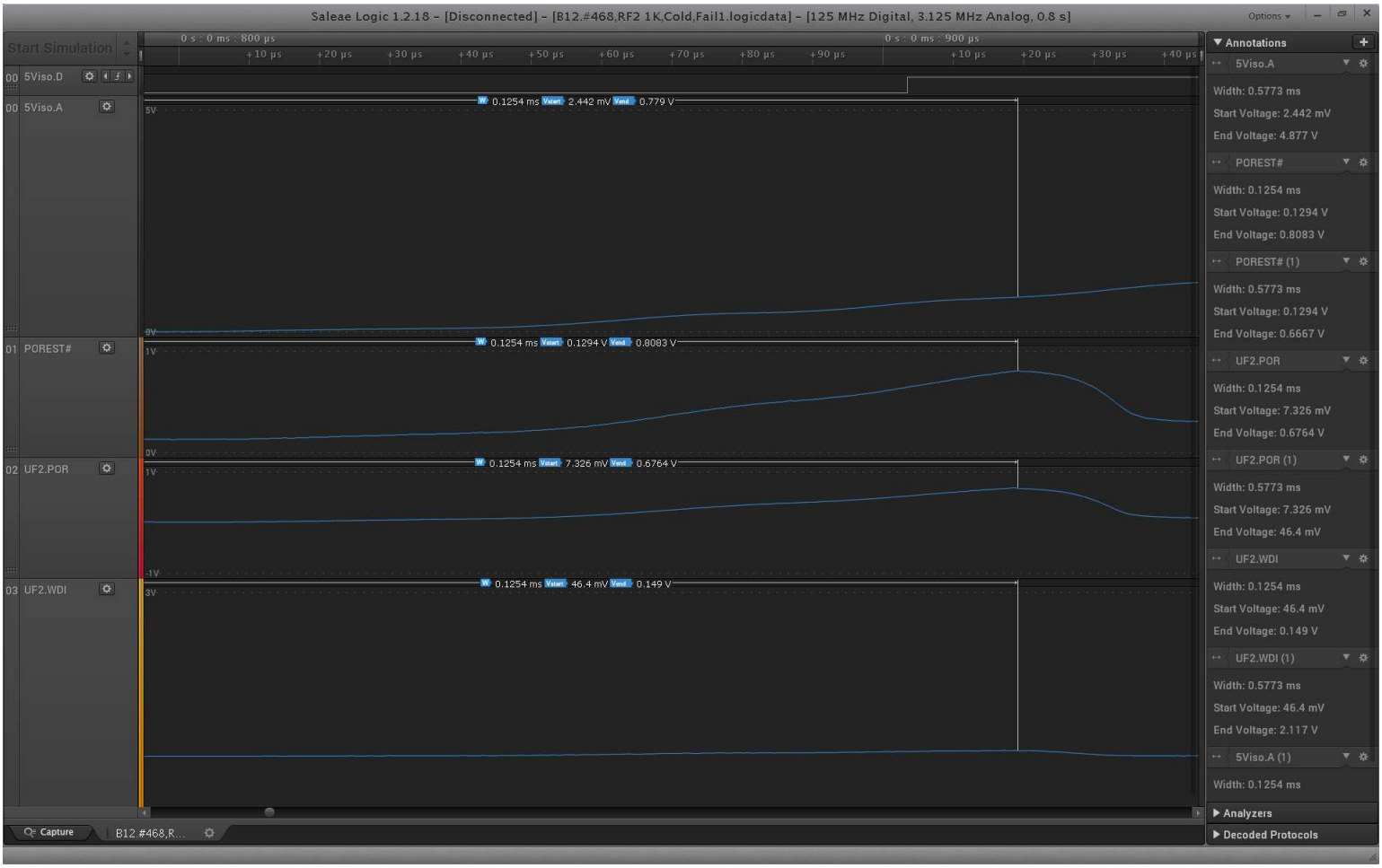


Figure 6 Pass Cold Boot RF0 = 1K

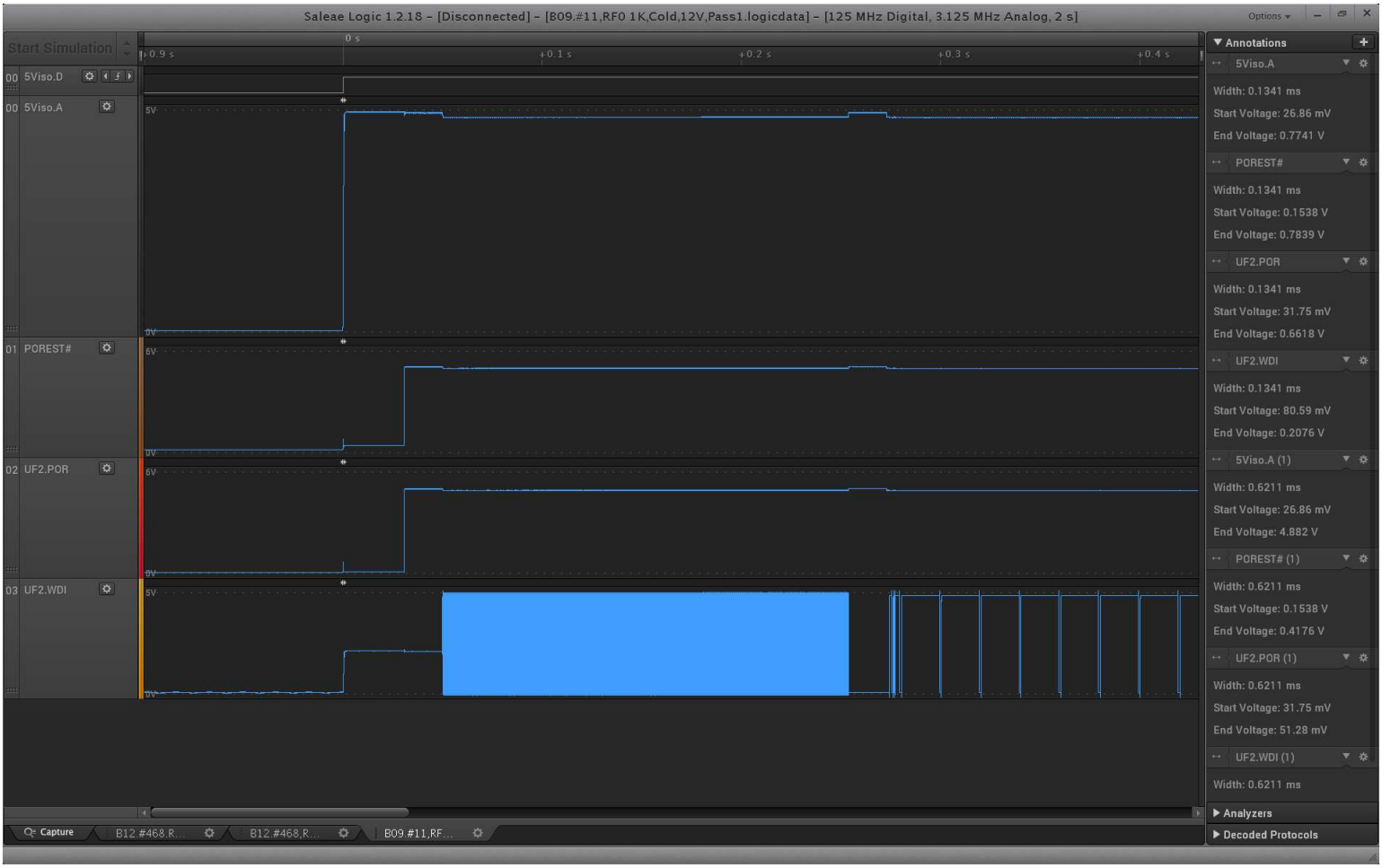


Figure 7 Pass Cold Boot RF0 = 1K Zoom 1

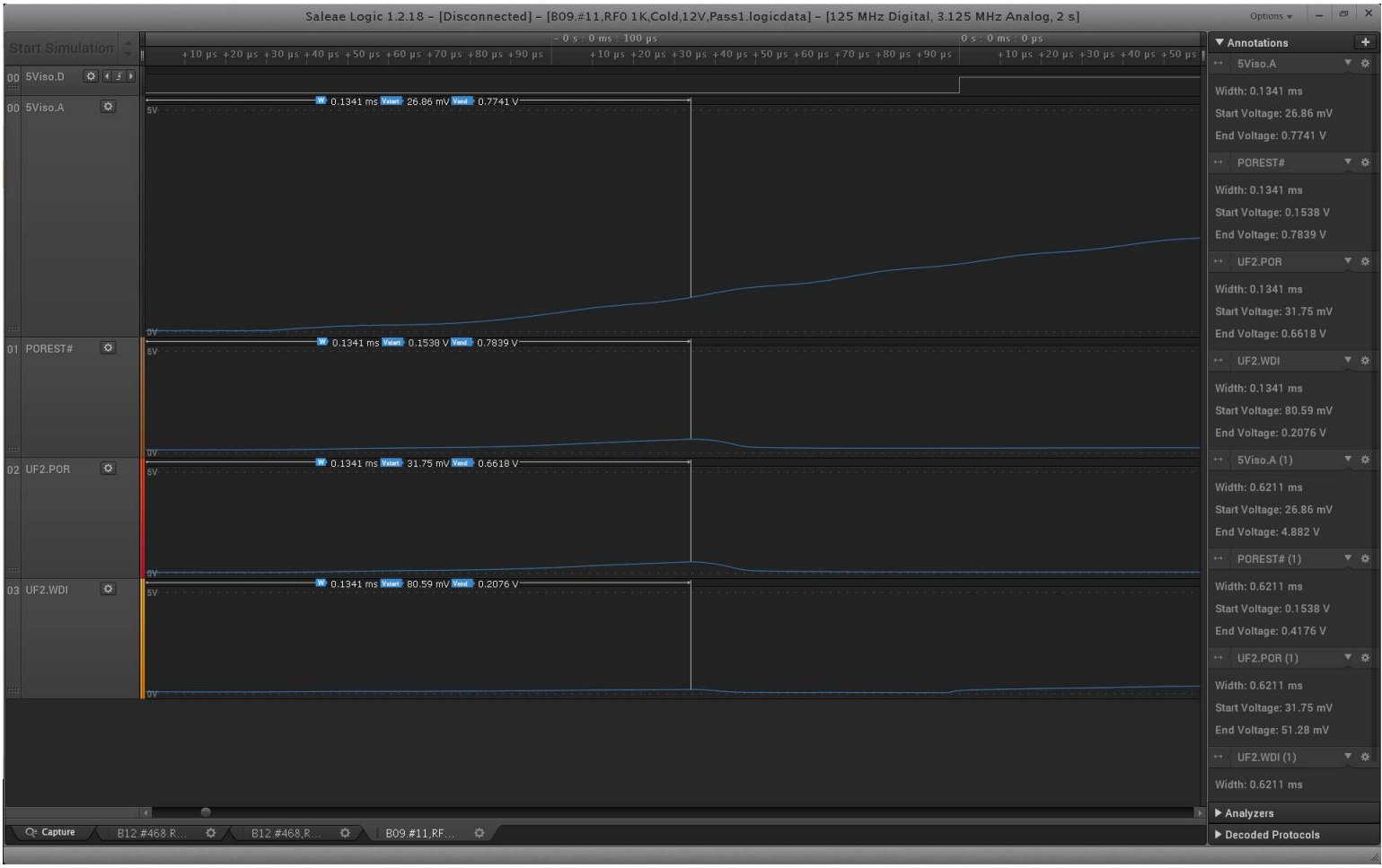
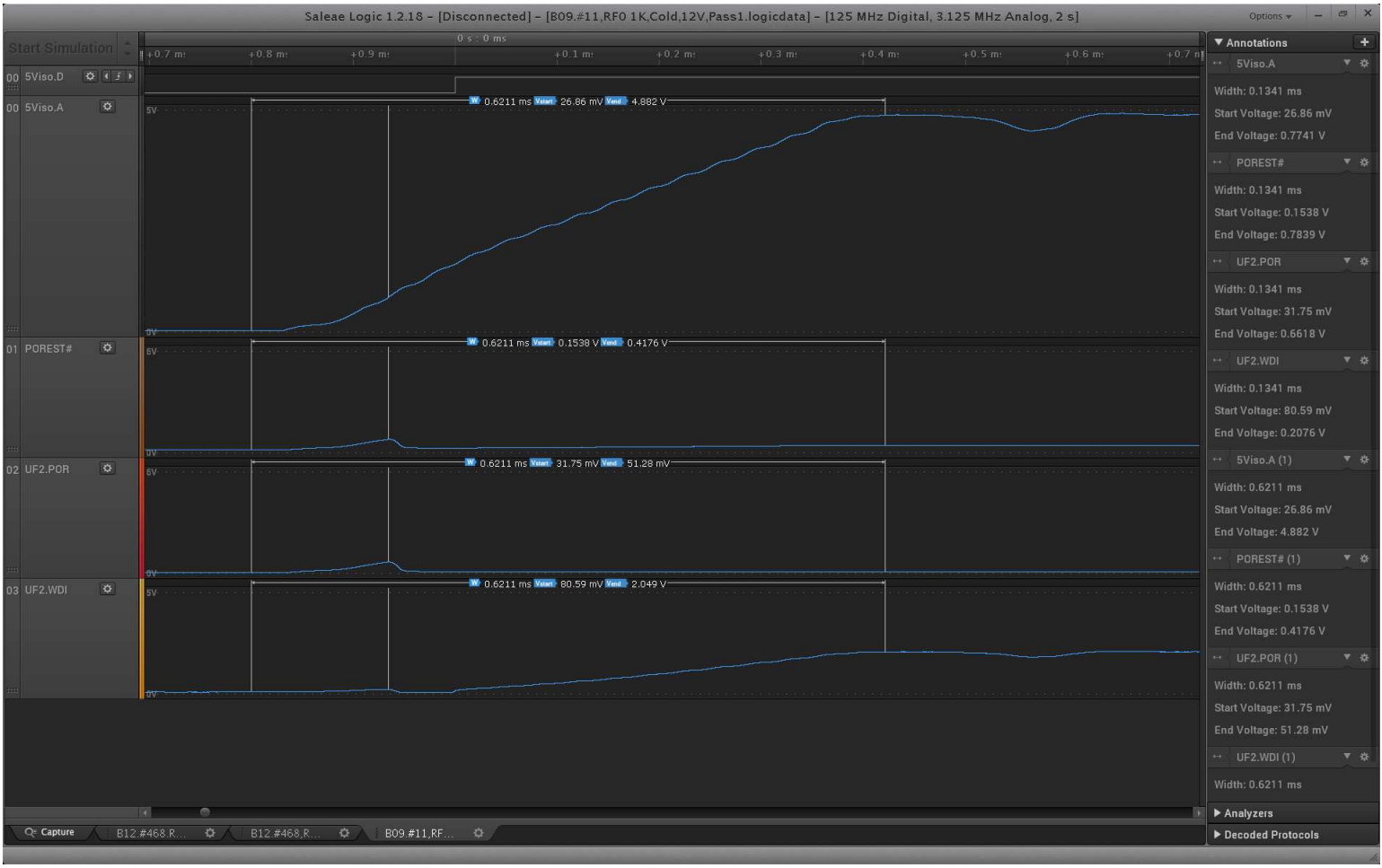


Figure 8 Pass Cold Boot RF0 = 1K Zoom 2


Saleae Logic 1.2.18 – [Disconnected] – [B09.#11,RF0 1K,Cold,12V,Pass1.logicdata] – [125 MHz Digital, 3.125 MHz Analog, 2 s]
Options
Start Simulation
0 s : 0 ms
+0.7 m:
+0.8 m:
+0.9 m:
+0.1 m:
+0.2 m:
+0.3 m:
+0.4 m:
+0.5 m:
+0.6 m:
+0.7 m:
00 5Viso.D
00 5Viso.A
01 POREST#
02 UF2.POR
03 UF2.WDI
5V
0V
W 0.6211 ms Vstart 26.86 mV Vend 4.882 V
W 0.6211 ms Vstart 0.1538 V Vend 0.4176 V
W 0.6211 ms Vstart 31.75 mV Vend 51.28 mV
W 0.6211 ms Vstart 80.59 mV Vend 2.049 V
Capture
B12.#468,R...
B12.#468,R...
B09.#11,RF...
Annotations
5Viso.A
Width: 0.1341 ms
Start Voltage: 26.86 mV
End Voltage: 0.7741 V
POREST#
Width: 0.1341 ms
Start Voltage: 0.1538 V
End Voltage: 0.7839 V
UF2.POR
Width: 0.1341 ms
Start Voltage: 31.75 mV
End Voltage: 0.6618 V
UF2.WDI
Width: 0.1341 ms
Start Voltage: 80.59 mV
End Voltage: 0.2076 V
5Viso.A (1)
Width: 0.6211 ms
Start Voltage: 26.86 mV
End Voltage: 4.882 V
POREST# (1)
Width: 0.6211 ms
Start Voltage: 0.1538 V
End Voltage: 0.4176 V
UF2.POR (1)
Width: 0.6211 ms
Start Voltage: 31.75 mV
End Voltage: 51.28 mV
UF2.WDI (1)
Width: 0.6211 ms
Analyzers
Decoded Protocols