NOTE
THESE SIGNALS ARE 5V CMOS LOGIC INPUTS
AND MUST BE DRIVEN BY 5V SIGNALS

5 IOSERI_CLK
5,13 IOSER_LD

IOSERO_CLK
IOSER_CLR#
IOSER_LD

DOUT31 SHIFTS IN FIRST
5 IOSER_OUT
C317 10pF/50V/NPO

LAYOUT:
DOUT[0..31] ARE
50V 1Amp TRACKS

RESET# LOW CLEARS ALL REGISTERS
INPUT LATCHED IN ON SCLK FALLING
OUTPUTS LOADED ON CE RISING
OUTPUT STATUS LATCHED ON CE FALLING
SO TRANSITIONS AFTER SCLK RISING
SO 3-STATE WHEN CE HIGH
"1" DATA TURNS OFF OUTPUT
SCLK SHOULD BE LOW WHEN CE HIGH

IOSERI_CLK R78 10K/1%
IOSERO_CLK R125 10K/1%
IOSER_OUT R127 10K/1%
IOSER_LD R77 10K/1%
IOSER_CLR# R126 10K/1%

R58 10K/1%

U2 U3 U4 U8 U11 U7 U6 U10
SERIN A B C D E F G H QH QH
CLK INH SH/LD VCC VSS
TI_SN74HC165DR

RN1 RN2 RN3 RN4 RN5 RN6 4.7KX4/5%
RN7 RN8 RN9 RN10 RN11 RN12 RN13 RN14 RN15 RN16 47KX4/5%

DIN0 DIN1 DIN2 DIN3 DIN4 DIN5 DIN6 DIN7
DIN8 DIN9 DIN10 DIN11 DIN12 DIN13 DIN14 DIN15
DIN16 DIN17 DIN18 DIN19 DIN20 DIN21 DIN22 DIN23
DIN24 DIN25 DIN26 DIN27 DIN28 DIN29 DIN30 DIN31

C213 10uF/10V/X5R
C212 C215 C216 C214 C228 0.1uF/16V/X5R

R74 22R/5%
IOSER_IN 5

NOTE
THIS SIGNAL IS 5V CMOS OUTPUT

C231 10pF/50V/NPO
C232 10pF/50V/NPO

LAYOUT NOTE:
PLACE THESE CAPACITORS
AT END OF SIGNAL TRACK

C312 10pF/50V/NPO
C314 10pF/50V/NPO
C313 10pF/50V/NPO

LAYOUT NOTE:
PLACE THESE CAPACITORS
AT END OF SIGNAL TRACK

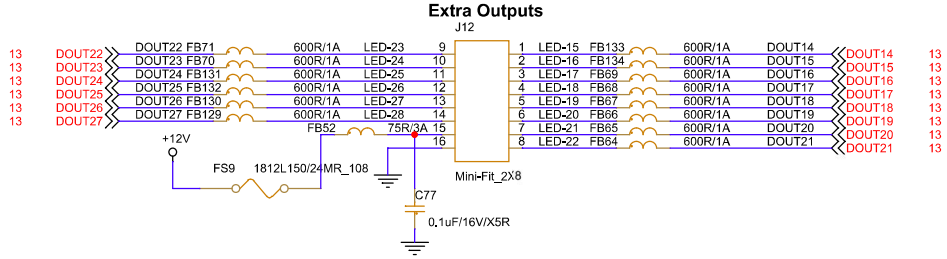
SER_IN SRCK SRCLR# RCK G# SER_OUT
DRAIN0 DRAIN1 DRAIN2 DRAIN3 DRAIN4 DRAIN5 DRAIN6 DRAIN7
PGND VCC LGND
TI_TPIC6A596DW

C316 C318 C221 C222 C223 C224 C315 0.1uF/16V/X5R
C318 C222 C224 10uF/10V/X5R

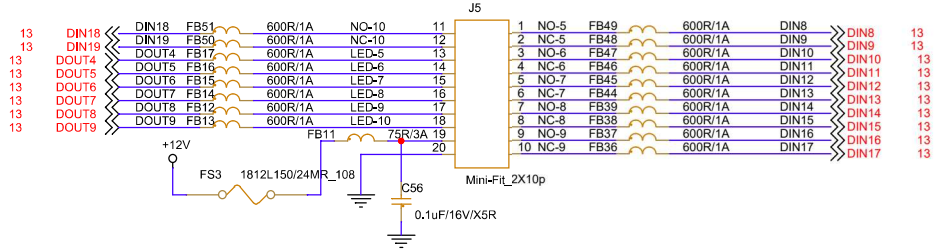
DOUT0 DOUT1 DOUT2 DOUT3 DOUT4 DOUT5 DOUT6 DOUT7
DOUT8 DOUT9 DOUT10 DOUT11 DOUT12 DOUT13 DOUT14 DOUT15
DOUT16 DOUT17 DOUT18 DOUT19 DOUT20 DOUT21 DOUT22 DOUT23
DOUT24 DOUT25 DOUT26 DOUT27 DOUT28 DOUT29 DOUT30 DOUT31

Type something…

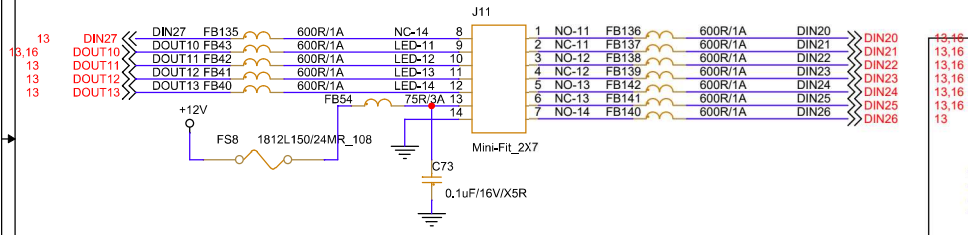
Extra Outputs



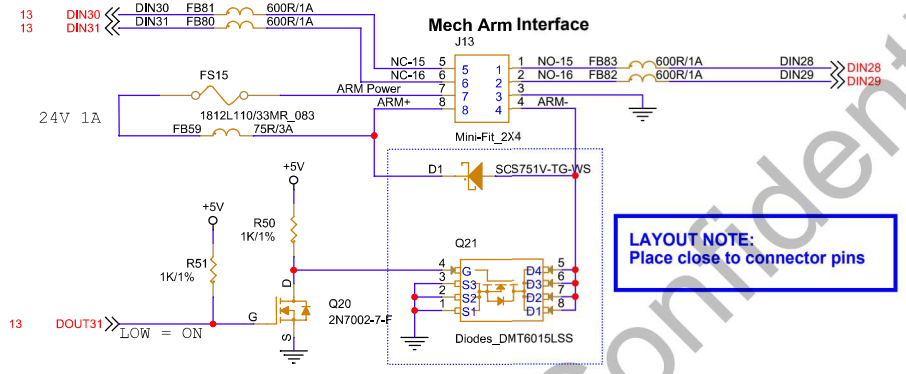
6 Button Interface



4 Button Interface

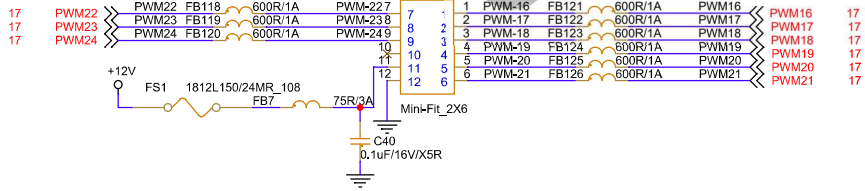


Mech Arm Interface



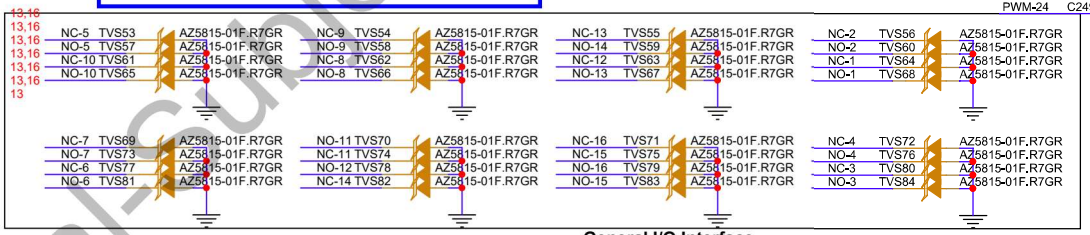
LAYOUT NOTE:
Place close to connector pins

PWM-2

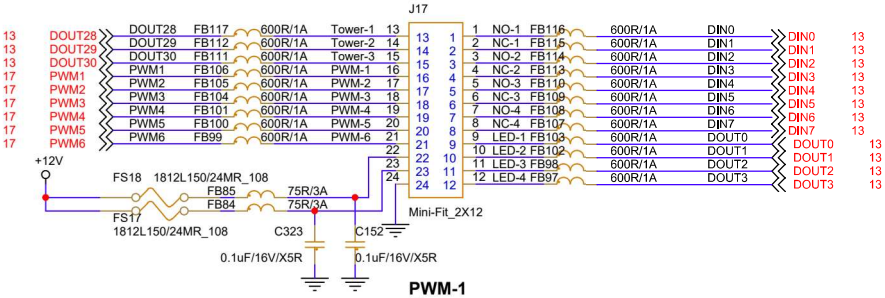


LAYOUT NOTE:
All capacitors to be placed as close as possible to connector pins

LAYOUT NOTE:
TVS - All nets swapable within device and between devices. Place close to connector pins



General I/O Interface



PWM-1