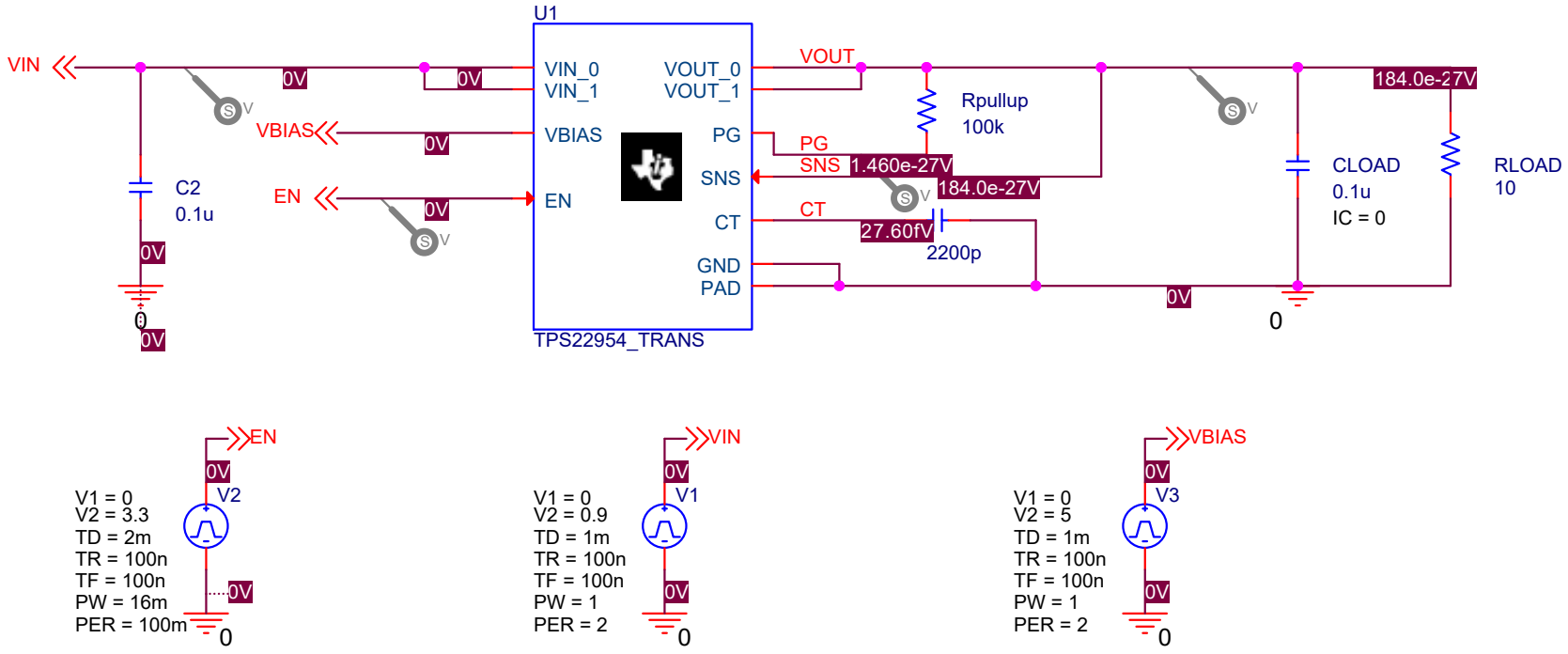
TPS22954 START-UP SIMULATION

Title	TPS2295x 5.7-V, 5-A, 16-mO On-Resistance Load Switch	
Size: Custom	Document Number: Datasheet:SLVSCT55 –NOV 2014	Rev: 1.0
Date: Monday, March 08, 2021	Sheet 1 of 1	



Application Notes:

1. The PSpice macromodel for TPS22954 is unencrypted and will only run in PSPICE Versions 15.7 and up.
2. The test bench has been configured for VIN=2.5V, VOUT=2.5V,and IOUT=250mA to record timing characterstics for different set of VIN and VBIAS value.
3. Click PSpice ---> Run (F11) to run the simulation. The simulation runs for 10ms and takes ~ 1 minute to run on 2.4GHz machine.
4. Thermal effect related chracteristic of the model have not modeled.

** Profile: "TPS22954_STARTUP-VINVDDP" [D:¥AMD Embbeded¥Devices¥DC-DC¥PSpice for TI¥TPS22954_TEST¥tps22954_trans_vddp-pspicefiles¥

**** CIRCUIT DESCRIPTION

****

** Creating circuit file "VINVDDP.cir"
** WARNING: THIS AUTOMATICALLY GENERATED FILE MAY BE OVERWRITTEN BY SUBSEQUENT SIMULATIONS

*Libraries:
* Profile Libraries :
* Local Libraries :
* From [PSPICE NETLIST] section of C:¥Users¥DevMan¥AppData¥Roaming¥SPB_Data¥cdssetup¥OrCAD_PSpiceTIPSpice_Install¥17.4.0¥PSpice.ini file:
.lib "nom_pspti.lib"
.lib "nom.lib"

```
*Analysis directives:
.TRAN    0 20m 0 100n
.OPTIONS ADVCONV
.PROBE64 V(alias(*)) I(alias(*)) W(alias(*)) D(alias(*)) NOISE(alias(*))
.INC "..¥TPS22954_STARTUP.net"



**** INCLUDING TPS22954_STARTUP.net ****
* source TPS22954_TRANS_VDDP
V_V1            VIN 0
+PULSE 0 0.9 1m 100n 100n 1 2
V_V2            EN 0
+PULSE 0 3.3 2m 100n 100n 16m 100m
V_V3            VBIAS 0
+PULSE 0 5 1m 100n 100n 1 2
R_RLOAD             0 SNS    10 TC=0,0
C_C2            0 VIN    0.1u    TC=0,0
R_Rpullup           PG SNS    100k TC=0,0
C_CLOAD             SNS 0    0.1u IC=0 TC=0,0
C_C1            CT 0    2200p
X_U1            CT EN PG SNS VIN VIN SNS SNS 0 VBIAS 0 TPS22954_TRANS
```

**** RESUMING VINVDDP.cir ****
.END

**** 03/09/21 08:10:04 ******* PSpice 17.4.0 (Nov 2018) ******* ID# 0 ********

** Profile: "TPS22954_STARTUP-VINVDDP" [D:¥AMD Embbeded¥Devices¥DC-DC¥PSpice for TI¥TPS22954_TEST¥tps22954_trans_vddp-pspicefiles¥

**** Diode MODEL PARAMETERS

****

	DD	X_U1.X_U1_U3_U789.DD
IS	1.000000E-15	1.000000E-15
N	.01	.01
TT	10.000000E-12	10.000000E-12

	X_U1.X_U1_U3_U787.DD
IS	1.000000E-15

N .01

TT 10.000000E-12

**** 03/09/21 08:10:04 ******* PSpice 17.4.0 (Nov 2018) ******* ID# 0 ********

** Profile: "TPS22954_STARTUP-VINVDDP" [D:¥AMD Embbeded¥Devices¥DC-DC¥PSpice for TI¥TPS22954_TEST¥tps22954_trans_vddp-pspicefiles¥

**** MOSFET MODEL PARAMETERS

****

NMOS01
NMOS
LEVEL 1
L 100.000000E-06
W 100.000000E-06
VTO .4
KP 9.8
GAMMA 0

PHI	.6
LAMBDA	1.000000E-03
IS	10.000000E-15
JS	0
PB	.8
PBSW	.8
CJ	0
CJSW	0
CGSO	0
CGDO	0
CGBO	0
TOX	0
XJ	0
UCRIT	10.000000E+03
DIOMOD	1
VFB	0
LETA	0
WETA	0
U0	0
TEMP	0
VDD	5
XPART	0

**** 03/09/21 08:10:04 ******* PSpice 17.4.0 (Nov 2018) ******* ID# 0 ********

** Profile: "TPS22954_STARTUP-VINVDDP" [D:¥AMD Embbeded¥Devices¥DC-DC¥PSpice for TI¥TPS22954_TEST¥tps22954_trans_vddp-pspicefiles¥

**** Voltage Controlled Switch MODEL PARAMETERS

****

X_U1.X_U1_U3_S2._U1_U3_S2

RON	1.000000E+09
ROFF	800
VON	.5
VOFF	.2

X_U1.X_U1_U1_S1._U1_U1_S1

RON 1.000000E-03
ROFF 100.000000E+06
VON .8
VOFF .2

X_U1.X_U1_U1_S2._U1_U1_S2
RON 1.000000E-03
ROFF 100.000000E+06
VON .8
VOFF .2

X_U1.X_U1_U2_S3._U1_U2_S3
RON 1.000000E-03
ROFF 100.000000E+06
VON .49
VOFF .51

X_U1.X_U1_U2_S4._U1_U2_S4
RON 100.000000E+06
ROFF 1.000000E-03

VON	.49
VOFF	.51

X_U1.X_U1_U2_S2._U1_U2_S2

RON	1
ROFF	1.000000E+09
VON	.2
VOFF	.8

**** 03/09/21 08:10:04 ******* PSpice 17.4.0 (Nov 2018) ******* ID# 0 ********

** Profile: "TPS22954_STARTUP-VINVDDP" [D:¥AMD Embbeded¥Devices¥DC-DC¥PSpice for TI¥TPS22954_TEST¥tps22954_trans_vddp-pspicefiles¥

**** INITIAL TRANSIENT SOLUTION TEMPERATURE = 27.000 DEG C

****

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(CT) 27.60E-15 (EN) 0.0000 (PG) 1.460E-27 (SNS) 184.0E-27

(VIN) 0.0000 (VBIAS) 0.0000 (X_U1.VIN) 0.0000

(X_U1.U1_U1_K0) 1.0000 (X_U1.U1_U1_K1) 1.0000

(X_U1.N14554815) 0.0000 (X_U1.N14557626) 184.0E-27

(X_U1.U1_N02574) 0.0000 (X_U1.U1_U2_VGI) 0.0000

(X_U1.U1_U2_GC_H) 0.0000 (X_U1.U1_U2_GC_L) 0.0000

(X_U1.U1_U2_V0P7) 0.0000 (X_U1.U1_U2_V1P2) 0.0000

(X_U1.U1_U2_V1P5) 0.0000 (X_U1.U1_U2_V1P8) 0.0000

(X_U1.U1_U2_V2P5) 0.0000 (X_U1.U1_U2_V3P3) 0.0000

(X_U1.U1_U2_V5P0) 0.0000 (X_U1.ON_INT_PRE1) 0.0000

(X_U1.U1_U1_N00239) .7000 (X_U1.U1_U1_N00271) .1000

(X_U1.U1_U1_VB_2P5) 0.0000 (X_U1.U1_U1_VB_5P0) 0.0000

(X_U1.U1_U2_VBIAS1) 0.0000 (X_U1.U1_U2_VBIAS2) 0.0000

(X_U1.U2_N14553136) 0.0000 (X_U1.U2_N14553152) 0.0000

(X_U1.U2_N14553232) 0.0000 (X_U1.U2_N14553248) 0.0000

(X_U1.U2_N14554177)	0.0000	(X_U1.U2_N14554193)	0.0000
(X_U1.U2_N14554279)	0.0000	(X_U1.X_U1_U1_U1.1)	0.0000
(X_U1.X_U1_U1_U2.1)	0.0000	(X_U1.U1_U1_N427858)	10.00E-12
(X_U1.U1_U1_N427908)	1.0000	(X_U1.U1_U1_N427944)	0.0000
(X_U1.U1_U1_N427964)	1.0000	(X_U1.U1_U1_VON_2P5)	0.0000
(X_U1.U1_U1_VON_5P0)	0.0000	(X_U1.U1_U2_VIN_INT)	0.0000
(X_U1.U1_SNS_INT_PRE)	0.0000	(X_U1.X_U1_U2_U9.106)	27.60E-15
(X_U1.X_U1_U2_U9.301)	276.0E-24	(X_U1.U1_U1_N14507001)	2.0000
(X_U1.U1_U1_N15077615)	0.0000	(X_U1.U1_U1_N16216534)	0.0000
(X_U1.U1_U1_N16219683)	0.0000	(X_U1.U1_U1_N16232344)	.5000
(X_U1.U1_U1_N16232358)	.0500	(X_U1.U1_U1_N16245251)	0.0000

(X_U1.U1_U2_N14501247)	0.0000	(X_U1.U1_U2_N14502461)	27.60E-15
(X_U1.U1_U2_N16248669)	0.0000	(X_U1.U1_U2_N16258419)	0.0000
(X_U1.U1_U2_N16258441)	0.0000	(X_U1.U1_U2_N16278616)	27.60E-15
(X_U1.U1_U2_N16284152)	0.0000	(X_U1.U1_U2_N16313138)	184.0E-27
(X_U1.U1_U2_N16318748)	0.0000	(X_U1.U1_U3_N14542417)	0.0000
(X_U1.U1_U3_N14542421)	1.0000	(X_U1.U1_U3_N14542517)	0.0000
(X_U1.U1_U3_N14542537)	1.0000	(X_U1.U1_U3_N14542599)	0.0000
(X_U1.U1_U3_N14542607)	0.0000	(X_U1.U1_U3_N14542635)	0.0000
(X_U1.U1_U3_N14542639)	0.0000	(X_U1.X_U1_U1_U1.INM1)	.7000
(X_U1.X_U1_U1_U1.INP1)	0.0000	(X_U1.X_U1_U1_U1.INP2)	0.0000
(X_U1.X_U1_U1_U2.INM1)	.5000	(X_U1.X_U1_U1_U2.INP1)	0.0000
(X_U1.X_U1_U1_U2.INP2)	0.0000	(X_U1.X_U1_U2_U10.106)	0.0000

(X_U1.X_U1_U2_U10.301) 184.0E-24 (X_U1.X_U1_U1_U43.YINT) 0.0000

(X_U1.X_U1_U1_U44.YINT) 0.0000 (X_U1.X_U1_U1_U46.YINT) 1.0000

(X_U1.X_U1_U3_U45.YINT) 0.0000 (X_U1.X_U1_U3_U46.YINT) 0.0000

(X_U1.X_U1_U3_U47.YINT) 0.0000 (X_U1.X_U1_U3_U787.INT) 72.49E-24

(X_U1.X_U1_U3_U789.INT) 72.49E-24 (X_U1.U1_U2_VGATE_CLAMP) 6.9000

(X_U1.X_U1_U3_U788.YINT) 1.0000 (X_U1.X_U1_U3_U790.YINT) 1.0000

(X_U1.X_U1_U3_U791.YINT1) 0.0000 (X_U1.X_U1_U3_U791.YINT2) 0.0000

(X_U1.X_U1_U3_U791.YINT3) 0.0000 (X_U1.X_U1_U3_U787.X_U1.YINT) 0.0000

(X_U1.X_U1_U3_U789.X_U1.YINT) 0.0000

(X_U1.X_U1_U3_U787.X_U22.YINT) 1.0000

(X_U1.X_U1_U3_U789.X_U22.YINT) 1.0000

(X_U1.X_U1_U3_U787.IN_B_DELAYED) 1.0000

(X_U1.X_U1_U3_U789.IN_B_DELAYED) 1.0000

VOLTAGE SOURCE CURRENTS

NAME	CURRENT
V_V1	1.380E-11
V_V2	0.000E+00
V_V3	0.000E+00
X_U1.V_VBIAS	0.000E+00
X_U1.V_V2	-9.202E-23
X_U1.V_U1_U1_V7	0.000E+00
X_U1.V_U1_U1_V5	-4.001E-12
X_U1.V_U1_U1_V6	0.000E+00
X_U1.V_U1_U1_V1	0.000E+00
X_U1.V_U1_U1_V3	0.000E+00
X_U1.V_U1_U1_V8	0.000E+00
X_U1.V_U1_U1_V4	-1.000E-08
X_U1.V_U1_U1_V2	0.000E+00

X_U1.V_U1_U2_VON 2.760E-22
X_U1.V_U1_U2_VIRPD 1.840E-22
X_U1.V_U2_VIN 0.000E+00
X_U1.V_V1 -1.380E-11
X_U1.X_U1_U2_U10.vsense 1.840E-22
X_U1.X_U1_U2_U9.vsense 2.760E-22

TOTAL POWER DISSIPATION 1.00E-08 WATTS

Reducing minimum delta to make the circuit converge.
Reducing minimum delta to make the circuit converge.
Reducing minimum delta to make the circuit converge.
Reducing minimum delta to make the circuit converge.
Reducing minimum delta to make the circuit converge.

ERROR(ORPSIM-15138): Convergence problem in Transient Analysis at Time = 1.000E-03.
Time step = 867.4E-21, minimum allowable step size = 1.000E-18

These voltages failed to converge:

V(CT) = 6.550V ¥ 21.44mV
V(X_U1.U1_U2_N14502461) = 6.550V ¥ 21.44mV
V(X_U1.U1_U2_N16278616) = 6.550V ¥ 21.44mV

V(X_U1.X_U1_U2_U9.106) = 6.550V ¥ 21.44mV

These supply currents failed to converge:

I(X_U1.E_U1_U2_E19) = -10.00GA ¥ -13.76pA
I(X_U1.X_U1_U2_U9.eout) = 0A ¥ 931.32pA
I(V_V1) = 828.02MA ¥ -853.00mA
I(X_U1.V_V2) = -65.50nA ¥ -211.98pA
I(X_U1.V_U1_U1_V5) = -4.001pA ¥ -5.301pA
I(X_U1.V_U1_U2_VON) = 65.50nA ¥ 214.35pA
I(X_U1.V_V1) = -828.02MA ¥ 892.67uA
I(X_U1.X_U1_U2_U9.vsense) = 0A ¥ 931.32pA

These devices failed to converge:
X_U1.D_U1_U2_D4 X_U1.D_U1_U2_D3 X_U1.E_U1_U2_E19 X_U1.M_U1_U2_M1

Last node voltages tried were:

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(CT) 6.5504 (EN) 0.0000 (PG) 413.6E-15 (SNS) 52.11E-12

(VIN) .4500 (VBIAS) 2.5000 (X_U1.VIN) .4500

(X_U1.U1_U1_K0) 1.0000 (X_U1.U1_U1_K1) 1.0000

(X_U1.N14554815) 2.5000 (X_U1.N14557626) 52.11E-12

(X_U1.U1_N02574) 0.0000 (X_U1.U1_U2_VGI) 1.929E-06

(X_U1.U1_U2_GC_H) 0.0000 (X_U1.U1_U2_GC_L) 0.0000

(X_U1.U1_U2_V0P7) 0.0000 (X_U1.U1_U2_V1P2) 0.0000

(X_U1.U1_U2_V1P5) 0.0000 (X_U1.U1_U2_V1P8) 0.0000

(X_U1.U1_U2_V2P5) 0.0000 (X_U1.U1_U2_V3P3) 0.0000

(X_U1.U1_U2_V5P0) 0.0000 (X_U1.ON_INT_PRE1) 0.0000

(X_U1.U1_U1_N00239) .7000 (X_U1.U1_U1_N00271) .1000

(X_U1.U1_U1_VB_2P5) 57.92E-06 (X_U1.U1_U1_VB_5P0) 57.21E-06

(X_U1.U1_U2_VBIAS1)	6.429E-06	(X_U1.U1_U2_VBIAS2)	-.0010
(X_U1.U2_N14553136)	2.0006	(X_U1.U2_N14553152)	2.5000
(X_U1.U2_N14553232)	0.0000	(X_U1.U2_N14553248)	0.0000
(X_U1.U2_N14554177)	.3601	(X_U1.U2_N14554193)	.4500
(X_U1.U2_N14554279)	.4500	(X_U1.X_U1_U1_U1.1)	0.0000
(X_U1.X_U1_U1_U2.1)	0.0000	(X_U1.U1_U1_N427858)	-57.91E-09
(X_U1.U1_U1_N427908)	1.0000	(X_U1.U1_U1_N427944)	0.0000
(X_U1.U1_U1_N427964)	1.0000	(X_U1.U1_U1_VON_2P5)	1.639E-06
(X_U1.U1_U1_VON_5P0)	1.864E-06	(X_U1.U1_U2_VIN_INT)	0.0000
(X_U1.U1_SNS_INT_PRE)	0.0000	(X_U1.X_U1_U2_U9.106)	6.5504
(X_U1.X_U1_U2_U9.301)	0.0000	(X_U1.U1_U1_N14507001)	2.0000

(X_U1.U1_U1_N15077615)	0.0000	(X_U1.U1_U1_N16216534)	57.92E-06
(X_U1.U1_U1_N16219683)	57.92E-06	(X_U1.U1_U1_N16232344)	.5000
(X_U1.U1_U1_N16232358)	.0500	(X_U1.U1_U1_N16245251)	1.639E-06
(X_U1.U1_U2_N14501247)	0.0000	(X_U1.U1_U2_N14502461)	6.5504
(X_U1.U1_U2_N16248669)	0.0000	(X_U1.U1_U2_N16258419)	52.11E-12
(X_U1.U1_U2_N16258441)	0.0000	(X_U1.U1_U2_N16278616)	6.5504
(X_U1.U1_U2_N16284152)	0.0000	(X_U1.U1_U2_N16313138)	52.11E-12
(X_U1.U1_U2_N16318748)	22.0000	(X_U1.U1_U3_N14542417)	0.0000
(X_U1.U1_U3_N14542421)	1.0000	(X_U1.U1_U3_N14542517)	0.0000
(X_U1.U1_U3_N14542537)	1.0000	(X_U1.U1_U3_N14542599)	0.0000
(X_U1.U1_U3_N14542607)	0.0000	(X_U1.U1_U3_N14542635)	0.0000
(X_U1.U1_U3_N14542639)	0.0000	(X_U1.X_U1_U1_U1.INM1)	.7000

(X_U1.X_U1_U1_U1.INP1) 0.0000 (X_U1.X_U1_U1_U1.INP2) 0.0000

(X_U1.X_U1_U1_U2.INM1) .5000 (X_U1.X_U1_U1_U2.INP1) 0.0000

(X_U1.X_U1_U1_U2.INP2) 0.0000 (X_U1.X_U1_U2_U10.106) 0.0000

(X_U1.X_U1_U2_U10.301) 2.368E-12 (X_U1.X_U1_U1_U43.YINT) 0.0000

(X_U1.X_U1_U1_U44.YINT) 0.0000 (X_U1.X_U1_U1_U46.YINT) 1.0000

(X_U1.X_U1_U3_U45.YINT) 0.0000 (X_U1.X_U1_U3_U46.YINT) 0.0000

(X_U1.X_U1_U3_U47.YINT) 0.0000 (X_U1.X_U1_U3_U787.INT) 70.91E-27

(X_U1.X_U1_U3_U789.INT) 70.91E-27 (X_U1.U1_U2_VGATE_CLAMP) 6.9000

(X_U1.X_U1_U3_U788.YINT) 1.0000 (X_U1.X_U1_U3_U790.YINT) 1.0000

(X_U1.X_U1_U3_U791.YINT1) 0.0000 (X_U1.X_U1_U3_U791.YINT2) 0.0000

(X_U1.X_U1_U3_U791.YINT3) 0.0000 (X_U1.X_U1_U3_U787.X_U1.YINT) 0.0000

(X_U1.X_U1_U3_U789.X_U1.YINT) 0.0000

(X_U1.X_U1_U3_U787.X_U22.YINT) 1.0000

(X_U1.X_U1_U3_U789.X_U22.YINT) 1.0000

(X_U1.X_U1_U3_U787.IN_B_DELAYED) 1.0000

(X_U1.X_U1_U3_U789.IN_B_DELAYED) 1.0000

**** Interrupt ****