



Pin Functions

PIN		I/O	DESCRIPTION
No.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the Application and Implementation section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the Application and Implementation section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the Adjustable Rise Time section for more information
7	VOUT	O	Switch output
8			
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the Layout Example section for layout guidelines

NOTE: The information below is provided as a guideline only and NOT a substitute for complete application related analysis obligations that reside with OEM. The information below is based on nominal values and conditions only (i.e. not based on any min/max limit) as stated by the TPS22965-Q1 data sheet. The nominal values and valid operating conditions for the TPS22965-Q1 device are specified in the device data sheet (Lit. Number SLVSCI3D), and are assumed to be completely followed in the instances in which normal device operation or no device damage is noted in the table below. If the user configures the TPS22965-Q1 device under any and all conditions presented by the data sheet's power inputs, loadings, recommended pin configurations, the concluding guidelines below are applicable and consistent.

Pin number	Name	Class	Short to Next Pin	Open Pin	Pin to GND
1,2 (internally shorted)	VIN	Input	(1&2→3) Device is always on if VIN > VIH. No damage to the device (1&2 → thermal pad) Device is disabled. Not functional. Damage may occur as high current flows from VIN to GND through the thermal pad and Silicon die.	Normal operation. However as VIN pin is open, no power is delivered to Vout if the switch is closed. No device damage.	Normal operation. However as VIN pin is GND, Vout is connected to GND through VIN pin if the switch is closed. No damage to the device.
3	ON	Input	(3→2) Device is always on if ON> VIH. No damage to the device. (3→4) Device is always on if VBIAS>VIH. No damage to the device. (3 → thermal pad) Device is disabled. Damage may occur as high current flows from ON to GND through the thermal pad and Silicon die.	Device could be on or off depending on ON pin voltage. No damage to the device.	Device is disabled. Not functional. No damage to the device.
4	VBIAS	Input	(4 → 3) Device is always on if ON> VIH. No damage to the device. (4 → thermal pad) Device is disabled. Not functional. Damage may occur as high current flows from ON to GND through the thermal pad and Silicon die.	No power supply to the device and the device not functional. The device will not pass through voltage to VOUT. No damage to the device.	Device is disabled. No damage to the device.
5	GND	GND	(5→6) Device will not turn on. No damage to the device. (5→thermal pad) Same as normal operation.	No GND connection to the device. Not functional. No damage to the device.	Normal operation. No damage to the device.
6	CT	Output	(6→7) CT pin can go as high as Vin+Vdiode or 18V if Vin is float with light load at Vout. Damage may occur due to high voltage at Vout pin. (6→thermal pad) Device is disabled. No damage to the device.	This will quicken the rise time comparing to the use case with a capacitor at the CT pin. No damage to the device.	Device is disabled. No damage to the device.
7,8 (internally shorted)	OUT	Output	(7&8→6) CT pin can go as high as Vin+Vdiode or 18V if Vin is float if there light load at Vout. Damage may occur. (7&8→thermal pad) Damage may occur because the power FET is turned on with output shorted to GND via the thermal pad and Silicon die.	The output will not deliver the voltage to the load. No damage to the device.	Damage may occur because the power FET is turned on with output shorted to GND.
-	Thermal Pad	-			