

Perliminary

Texas Instruments and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. Texas Instruments and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. Texas Instruments and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Orderable: No	Designed for: Public Release	Mod. Date: 4/24/2024
TID #: N/A	Project Title:	
Number:	Rev:	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 3
Drawn By: D.Xing	File: PMP23365B_1byback ver_SH1_SchDoc	Size: C
Engineer: D.Xing	Contact: N/A	



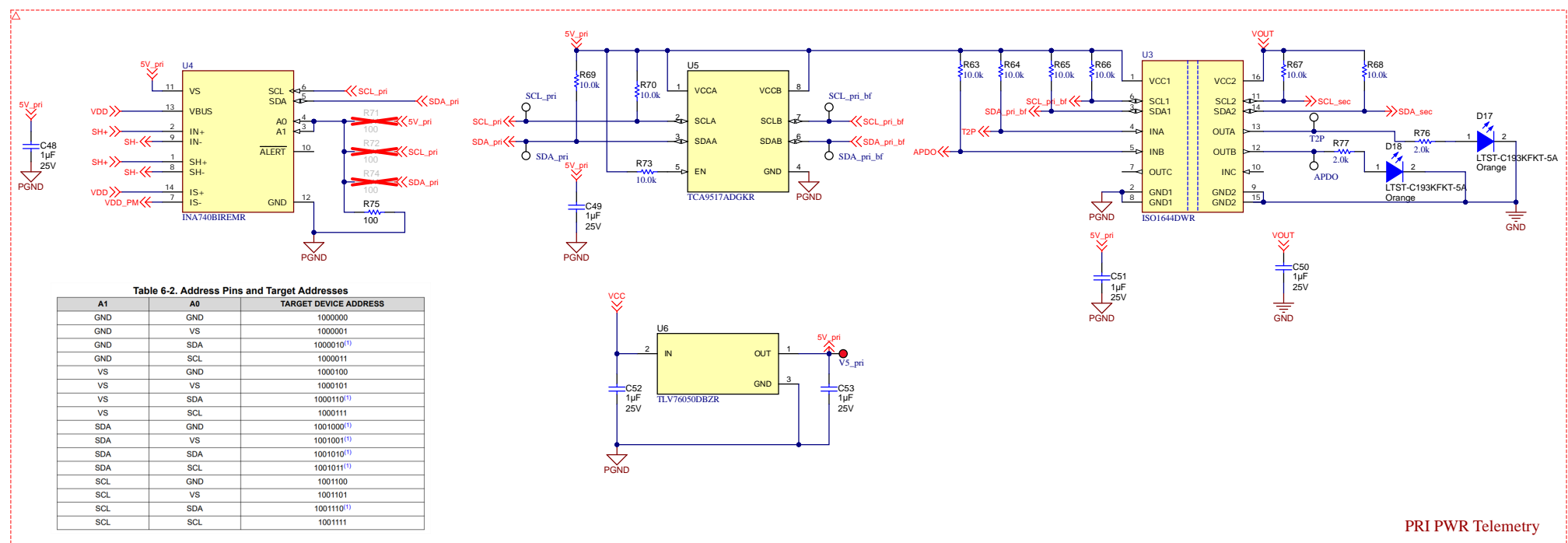
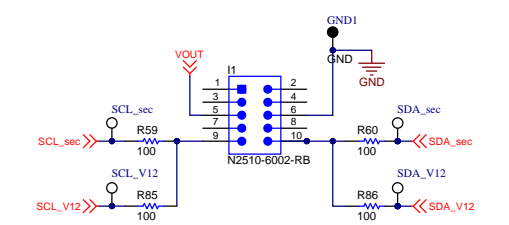
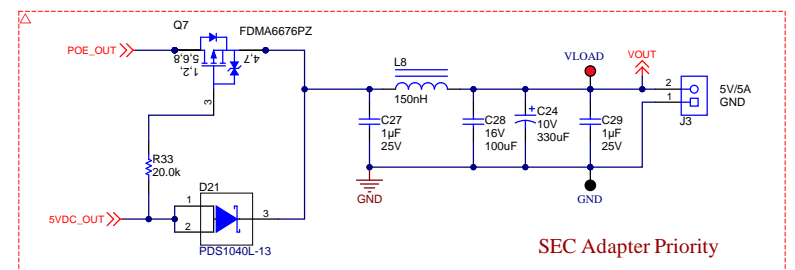
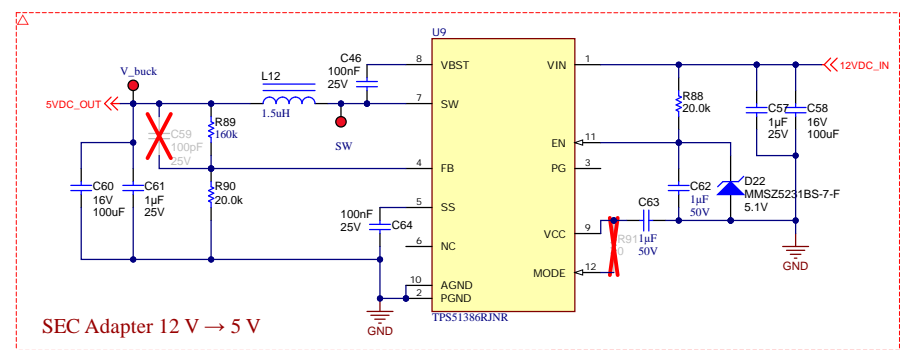
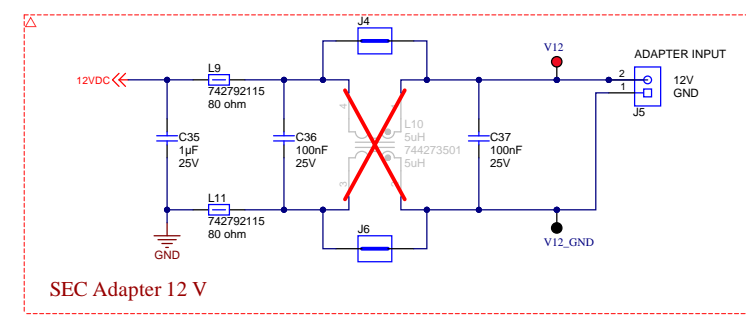
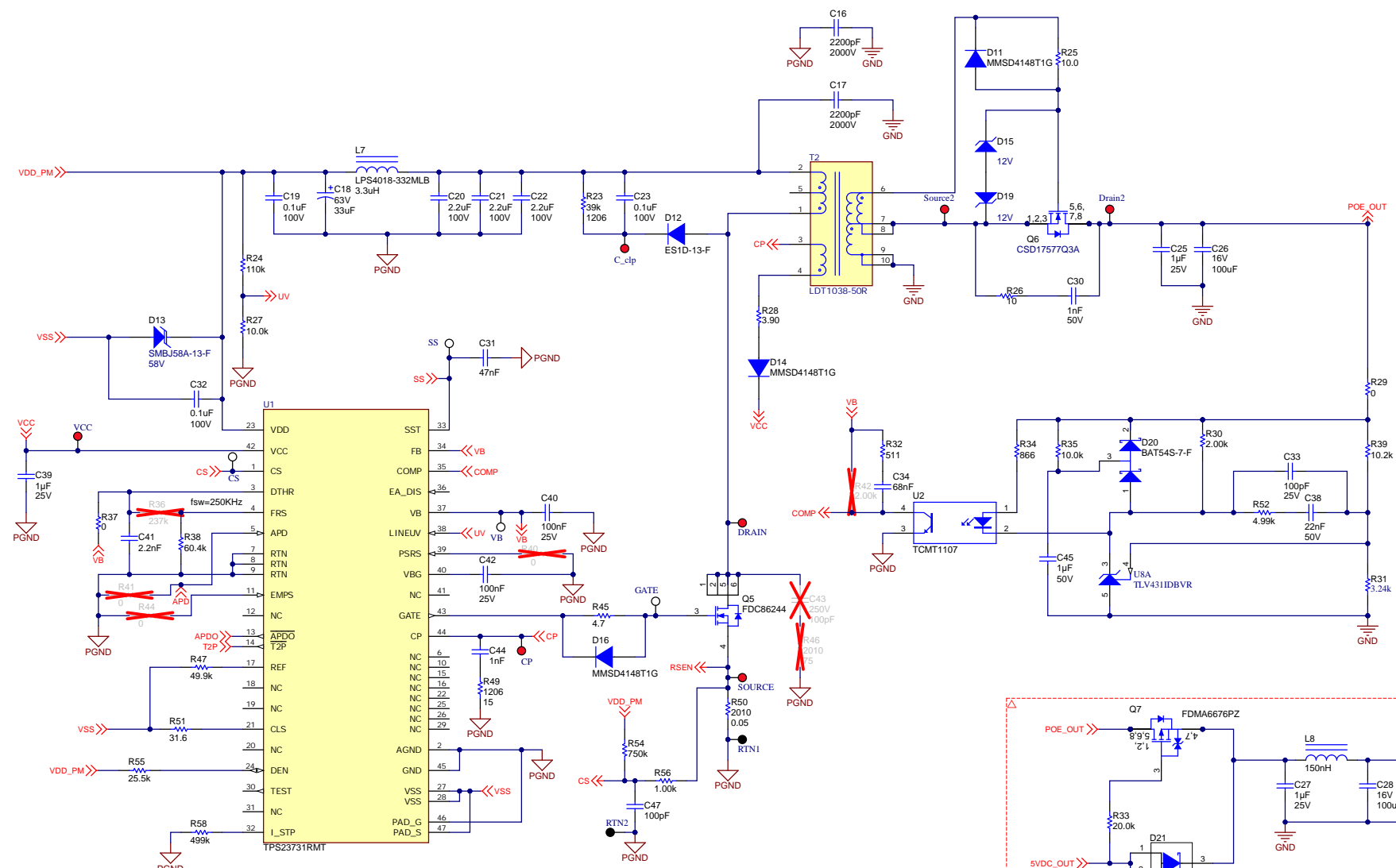


Table 6-2. Address Pins and Target Addresses

A1	A0	TARGET DEVICE ADDRESS
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010 ⁽¹⁾
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110 ⁽¹⁾
VS	SCL	1000111
SDA	GND	1001000 ⁽¹⁾
SDA	VS	1001001 ⁽¹⁾
SDA	SDA	1001010 ⁽¹⁾
SDA	SCL	1001011 ⁽¹⁾
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110 ⁽¹⁾
SCL	SCL	1001111

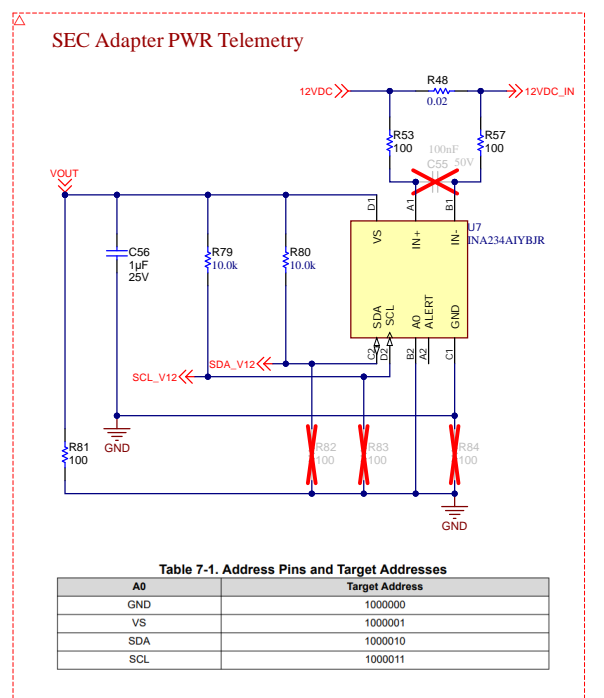


Table 7-1. Address Pins and Target Addresses

A0	Target Address
GND	1000000
VS	1000001
SDA	1000010
SCL	1000011

Perliminary