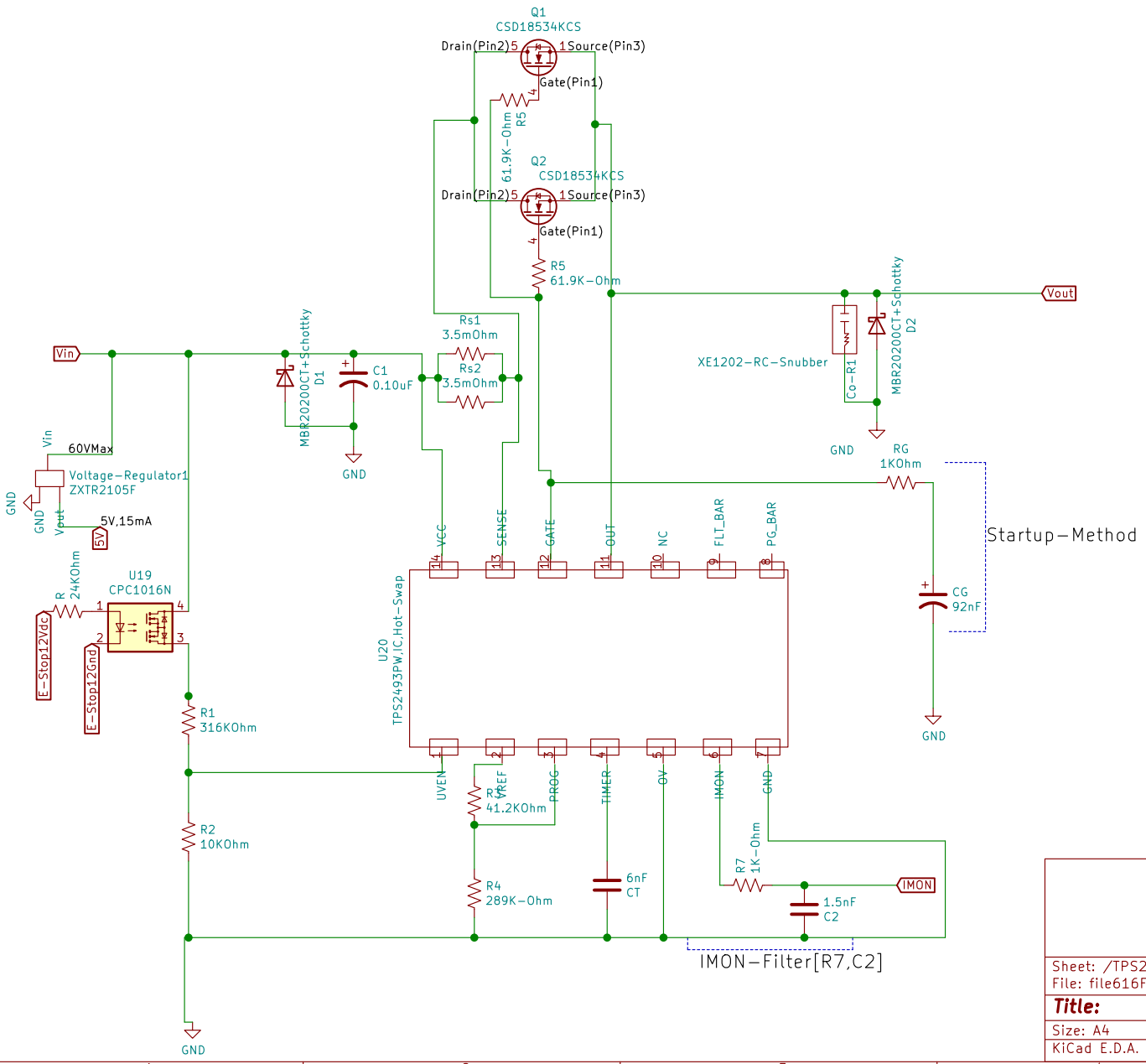
TPS2943 Soft-Starter for Driving Motor System Design



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
UVEN	1	I	A low input inhibits GATE. A logic input can drive this pin as an enable.
VREF	2	O	4-V reference voltage used to set the power threshold on PROG pin.
PROG	3	I	FET power-limit programming pin
TIMER	4	I/O	A capacitor from TIMER to ground sets the fault timer period.
OV	5	I	Overvoltage sensing input. A high input inhibits GATE.
IMON	6	O	Current monitor output, nominally V_{IMON} = 48 x ($V_{VCC-SENSE}$).
GND	7	PWR	Ground
$\overline{PG}$	8	O	Active low power good output. This is driven by $V_{VCC-SENSE}$.
$\overline{FLT}$	9	O	Active low fault indicator output. $\overline{FLT}$ indicates the fault timer has expired. $\overline{FLT}$ is reset by UVEN, UVLO, or automatic restart.
NC	10		No connect
OUT	11	I	FET source voltage (output) sensing pin. Gate is clamped to a diode drop below OUT.
GATE	12	O	Gate driver output for external FET.
SENSE	13	I	Current sensed as $V_{VCC-SENSE}$ and the FET V_{DS} as $V_{SENSE-OUT}$. For low FET V_{DS}, current limits at 50mV.
VCC	14	I	Input supply and current sense positive input

Input/Output Ports
*Vin ,
*Vout,
*Imon,
*E-stop12V,
*E-stop-GND,
*TPS2943-GND,
*5V

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