

## Texas Instruments Qualification Summary

Quality and reliability are built into TI's culture, with the goal of providing customers high quality products. TI's semiconductor technologies are developed with a minimum goal of fewer than 50 Failures in Time (FIT) at 100,000 Power-On-Hours at 105C junction temperature. TI builds simulations, accelerated testing, and robustness evaluations into the product development process. During the product development process, TI carefully assesses silicon process reliability, package reliability, and silicon/package interaction.

TI also evaluates manufacturability of the device to verify a robust silicon and assembly flow to enable continuity of supply to customers. Non-Automotive devices are qualified with industry standard test methodologies performed primarily to the intent of the Joint Electron Devices Engineering Council (JEDEC). TI qualifies new devices, significant changes, and product families based on JEDEC JESD47. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

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<b>Qualification summary for:</b>	<b>TPS2561ADRCR</b>
<b>Report date:</b>	<b>05/13/2022</b>

Stress	Reference	Min Lot Qty	Sample Size / Lot	Condition	Duration	Result
TC	JESD22-A104	3	25	Temperature Cycle -65/150C	500 Cycles	PASS
AC/UHAST	JESD22-A102/JESD22-A118	3	25	Autoclave 121C or Unbiased HAST 130C / 85% RH	96 Hours	PASS
HTSL	JESD22-A103	3	25	High Temp Storage Bake 150C	1000 Hours	PASS
THB/HAST	JESD22-A101/JESD22-A110	3	25	THB 85C/85%RH or HAST 130C/110C/85% RH	1000 Hours or 96 Hours	PASS
CDM	JESD22-C101	1	3	ESD - CDM	Classification	<a href="#">See datasheet</a>
HBM	JS-001	1	3	ESD - HBM	Classification	<a href="#">See datasheet</a>
HTOL	JESD22-A108	3	77	Life Test, 125C	1000 Hours	PASS

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Stress	Reference	Min Lot Qty	Sample Size / Lot	Condition	Duration	Result
LU	JESD78	1	3	Latch-up	Per JESD78	PASS
MSL	JEDEC J-STD-020E			Per JEDEC J-STD-020E	Classification	<a href="#">See datasheet</a>

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