Functional Safety Information

TPS25940-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS25940-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

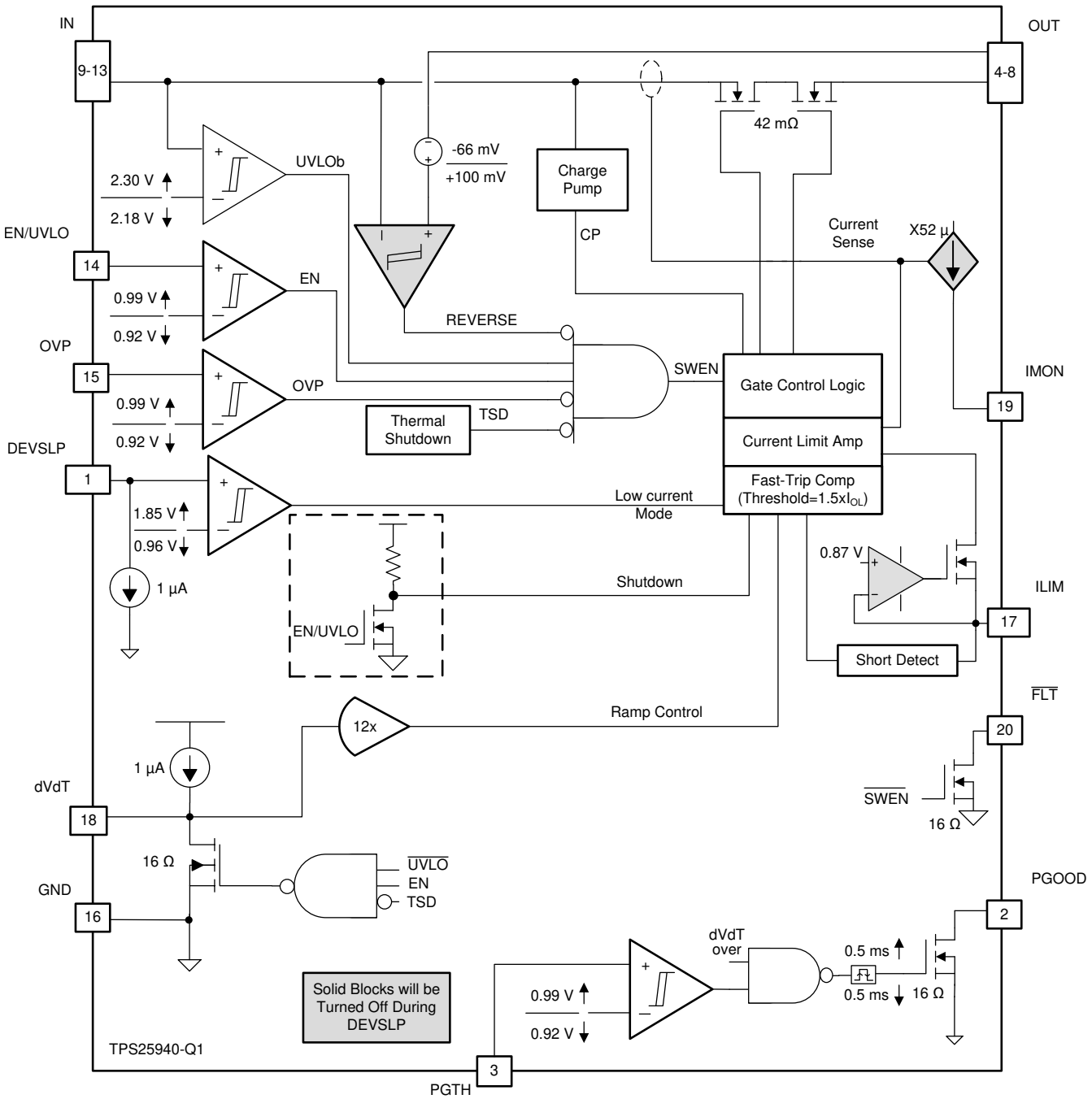

Figure 1-1. Functional Block Diagram

TPS25940-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS25940-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	16
Die FIT Rate	8
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 1000 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS25940-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Device fails to turn on (No output voltage)	25.98
Device functional but out of spec	24.88
Protection features compromised	23.81
Monitoring features compromised	25.33

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS25940-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-3)
- Pin open-circuited (see Table 4-2)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-3 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS25940-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS25940-Q1 data sheet.

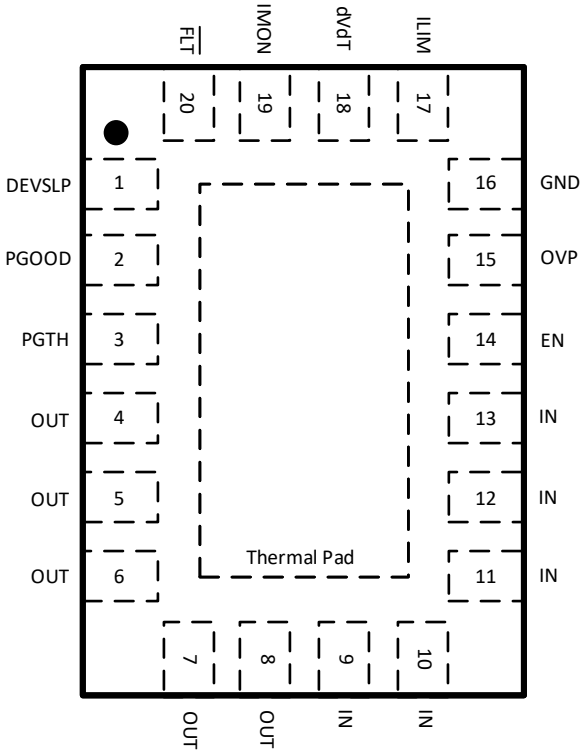

Figure 4-1. RVC Package 20-Pin WQFN Top View

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Unless otherwise specified, the voltage applied to the IN pins is within the TPS25940-Q1 Recommended Operating Range.

Table 4-2. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEVSLP	1	Device works normally.	D

Table 4-2. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
PGOOD	2	PGOOD indication not available. Otherwise device works normally.	B
PGTH	3	Threshold for power good assertion is not set correctly. Could lead to false power good assertion due to noise.	B
OUT	4, 5, 6, 7, 8	No power delivered to load.	B
IN	9, 10, 11, 12, 13	No supply to device. Device remains in powered down state.	B
EN	14	Device may not turn on.	B
OVP	15	Device may turn off due to noise.	B
GND	16	Device will turn off.	B
ILIM	17	Current limit is set to 450 mA.	B
dVdT	18	Device turns on with fastest slew rate.	B
IMON	19	Current monitor information not available, but normal operation otherwise.	B
/FLT	20	/FLT indication not available, but normal operation otherwise.	B
Thermal Pad		Poor thermal performance. Device may hit thermal shutdown at lower currents.	C

Table 4-3. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEVSLP	1	Device works normally.	D
PGOOD	2	PGOOD functionality is disabled and it remains permanently de-asserted.	B
PGTH	3	PGOOD signal will stay latched low, and can't be used downstream.	B
OUT	4, 5, 6, 7, 8	Short-circuit fast-trip protection is triggered and device turns off. Thereafter it remains latched-off (L variant) or performs auto-retry (A variant).	B
IN	9, 10, 11, 12, 13	Input supply short-circuit to ground. Device remains in power down state.	B
EN	14	Device remains turned off.	B
OVP	15	Overvoltage protection is disabled.	B
GND	16	Device works normally.	D
ILIM	17	Current limit is set to 670 mA.	B
dVdT	18	Device will not turn on.	B
IMON	19	Current monitor information not available, but normal operation otherwise.	B
/FLT	20	/FLT is permanently asserted, but normal operation otherwise.	B
Thermal Pad		Device works normally.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEVSLP	1	Once PGOOD is asserted, device goes into DEVSLEEP (low power mode), where it can deliver only 670mA to OUT.	B
PGOOD	2	PGOOD signal will stay latched low, and can't be used downstream.	B
PGTH	3	Threshold for power good assertion is equal to OUT voltage. Could lead to false power good assertion as soon as OUT voltage crosses 1V.	B
OUT	4	Device works normally.	D
OUT	5	Device works normally.	D
OUT	6	Device works normally.	D
OUT	7	Device works normally.	D
OUT	8	Device is bypassed. Input supply is delivered to output without any control or protection.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN	9	Device works normally.	D
IN	10	Device works normally.	D
IN	11	Device works normally.	D
IN	12	Device works normally.	D
IN	13	Device is always enabled when input supply is above UVLO threshold.	B
EN	14	Device will turn off.	B
OVP	15	Overvoltage protection is disabled.	B
GND	16	Current limit is set to 450 mA.	B
ILIM	17	Device can provide only < 10V and < 670mA to OUT. Soft-start feature will NOT work.	B
dVdT	18	If RIMON is used, OUT will get clamped to a small voltage (<2V), and no power available to downstream ICs. If no RIMON is used, soft-start feature of device will not work.	B
IMON	19	Current monitor information not available, but normal operation otherwise.	B
/FLT	20	/FLT is permanently asserted, but normal operation otherwise.	B
Thermal Pad		Refer to Table 4-3 for effect of each specific pin shorted to Thermal PAD (GND).	

Table 4-5. Pin FMA for Device Pins Short-Circuited to input supply (VIN)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
DEVSLP	1	Device goes into DEVSLEEP (low power mode), where it can deliver only 670mA to OUT.	B
PGOOD	2	If PGOOD signal is de-asserted by device, the internal pull down will provide low impedance path from supply to ground. The PGOOD pin will sink very large current and get damaged.	A
PGTH	3	Threshold for power good assertion is equal to supply voltage. Could lead to false power good assertion as soon as supply voltage crosses 1V.	B
OUT	4, 5, 6, 7, 8	Device is bypassed. Input supply is delivered to output without any control or protection.	B
IN	9, 10, 11, 12, 13	Device works normally.	D
EN	14	Device is always enabled when input supply is above UVLO threshold.	B
OVP	15	Device turns off.	B
GND	16	Input supply short-circuit to ground. Device remains in power down state.	B
ILIM	17	Current limit is set to very low value (nearly 0 A) and device will turn off if any load is applied to the output.	B
dVdT	18	Soft-start/inrush current limiting feature of device is disabled.	B
IMON	19	Current monitor information not reported correctly, but normal operation otherwise.	B
/FLT	20	If /FLT signal is asserted by device, the internal pull down will provide low impedance path from supply to ground. The /FLT pin will sink very large current and get damaged.	A
Thermal Pad		Input supply short-circuit to ground. Device remains in power down state.	B

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