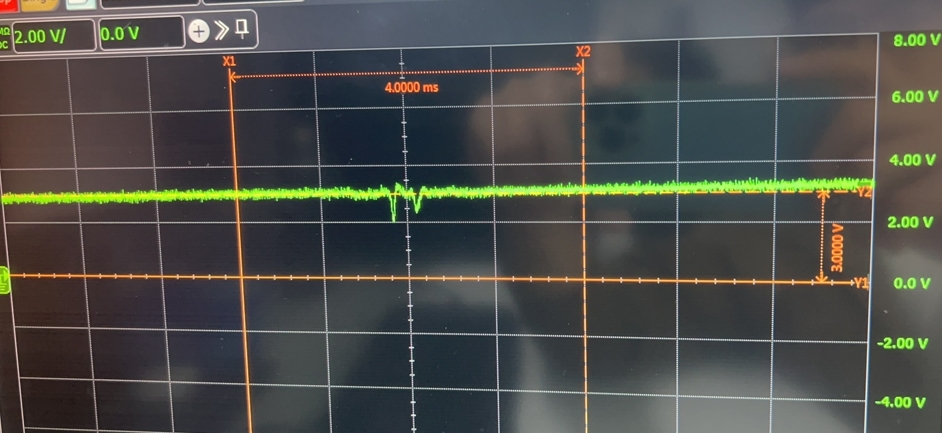
Updated 2023-12-13

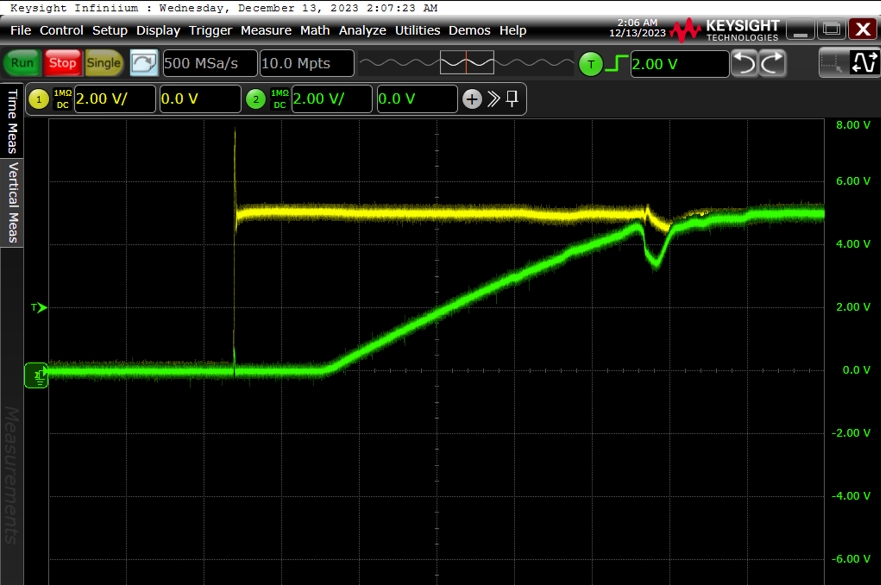
VCC5V and VDD1V0 are generated when they just reach the input voltage range, that is, the input range of TPS62130A is 3V~17V, and the voltage drop is generated when they just reach 3V.

No matter how the SS capacitor is adjusted, the voltage drop will occur when the load takes effect, so the measured modification of the SS pin capacitance does not have much impact.

Updated 2023-12-12

TPS25946 has done the following experiment, the effect is not obvious, please help to have a look, the results are as follows:

1. The output of TPS25946 or the input of TPS623130A (VDD1V0) is then connected in parallel with two 10uf capacitors (total capacity 30uf), and the voltage drop is changed from the original two to one, and the depth is not significantly changed, as shown in the figure below:



1. When the SS capacitance was modified to 4.7nf (FIG.1), 10nf (FIG. 2) and 47uf (FIG. 3), the position of voltage drop occurred earlier (in the middle of 2V~3.5V), 0.1uf was also tested and the previous email was replied. The experimental result of 0.5nf was similar to that of the suspended email, but the drop depth did not change significantly.

图形用户界面

描述已自动生成图形用户界面

描述已自动生成图形用户界面

描述已自动生成

1. The ILIM resistance was changed from the original 1.65k to 750Ω, and the drop depth did not change.

图形用户界面, 折线图

描述已自动生成

1. ITIMER did not weld the GND capacitor before. This time, 2.2nf was welded, and the voltage drop depth did not change.

图形用户界面

描述已自动生成

1. There are several small waves near the local amplified voltage drop, and the slope of the rest is monotonous. Is this loop instability?

图形用户界面

描述已自动生成

2023-12-07

The circuit design of TPS25946 and TPS62130A is as follows, and the following problems exist in the circuit measurement, please help to analyze the causes. (All the following tests did not stimulate the full plate power consumption, only the board is powered on, no system program) :图示

低可信度描述已自动生成

图形用户界面, 图示, 应用程序

描述已自动生成

1. a. VBUS5V (yellow line) will have voltage fluctuations about 5ms when powered on, see the waveform at the same position chip output VCC5V (green line) there are two voltage drops.图形用户界面

   描述已自动生成

b. The low voltage at the first place will cause the power on the rear circuit to have a step affecting the power-on sequence (the blue line is the PG signal at the rear stage), as shown in the figure below:

电脑显示屏

描述已自动生成

1. If the SS capacitor is deleted, that is, the SS pin is suspended, the voltage drop still exists, but the PG signal drop disappears.( VBUS5V- Yellow line, VCC5V- Green line, VDD1V8PG- Blue line)

电脑萤幕画面

描述已自动生成

At this time, a new problem is introduced, and the first power supply after VCC5V has a large fluctuation (only the first power supply appears, and the rest of the power supply after the stage does not appear, all use VCC5V as input, but the power-on timing is controlled through each chip PC: VDD1V0>VDD1V8>VDD2V5).

VCC5V- red line, VDD1V0-yellow line, VDD1V8-green line, VDD2V5- Blue line, locally enlarged as shown in the figure below:

电脑萤幕画面

描述已自动生成

图表

低可信度描述已自动生成

1. I use another brand of chip SGM40666, there is no voltage drop phenomenon.

（VBUS5V- Yellow line, VCC5V- green line）

图形用户界面, 应用程序, Excel

描述已自动生成