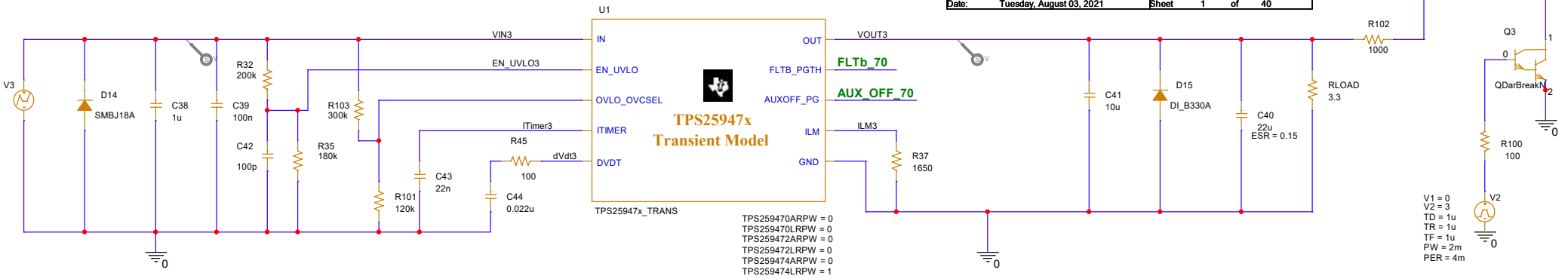
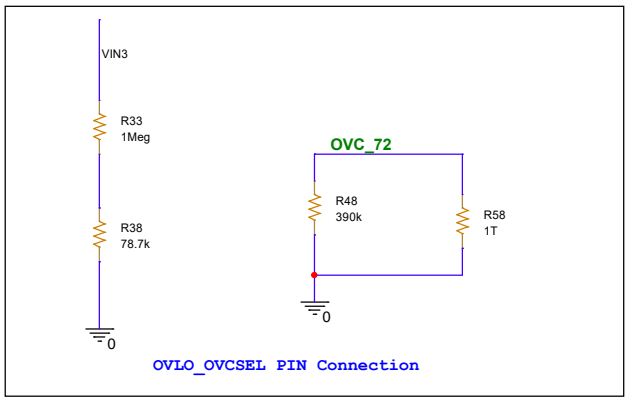
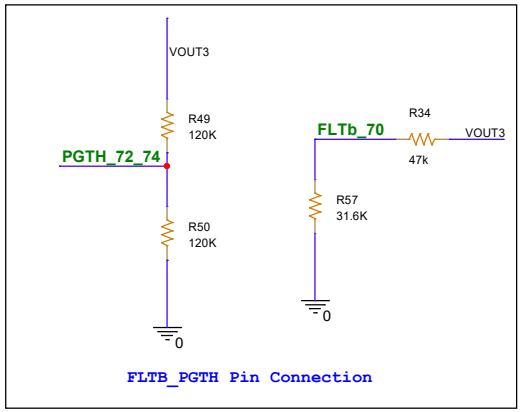
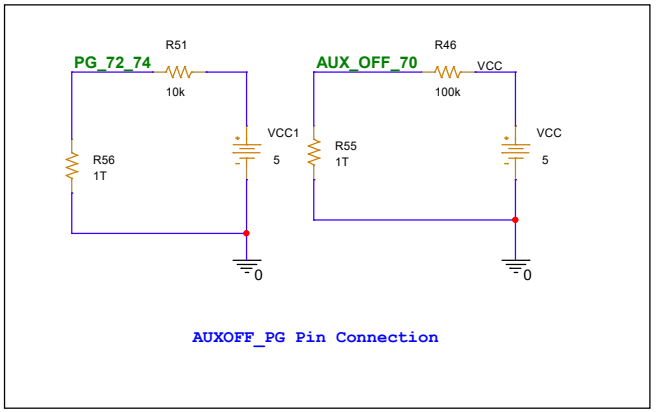
TPS25947x STARTUP SIMULATION

Title	TPS25947x: 2.7 - 23 V, 5.5 A, 28 mΩ True Reverse Current Blocking eFuse with Input Reverse Polarity Protection
Size A3	Document Number: Datasheet: SLVSFC9 EVM: SLVUC01 — Rev
Date: Tuesday, August 03, 2021	Sheet 1 of 40









Application Notes:

1. The TPS25947x model is encrypted and will only run in PSPICE Versions 17.2 and up.
3. The testbench has been configured Vin = 12V and Iout = 1A.
3. One among the 6 variants are selected by using the parameters
   - TPS259470LRPW=1--> TPS259470LRPW device is selected
   - TPS259470ARPW=1--> TPS259470ARPW device is selected
   - TPS259472LRPW=1--> TPS259472LRPW device is selected
   - TPS259472ARPW=1--> TPS259472ARPW device is selected
   - TPS259474LRPW=1--> TPS259474LRPW device is selected
   - TPS259474ARPW=1--> TPS259474ARPW device is selected
4. To select a particular variant set that parameter to 1 and rest to 0.
5. If TPS259470x is selected, connect
   - OVLO_70_74 --> OVLO pin
   - FLT_70 --> FLTB_PGTH pin
   - AUX_OFF_70 --> AUXOFF_PG pin

   If TPS259472x is selected, connect
   - OVC_72 --> OVCSEL pin
   - PGTH_72_74 --> FLTB_PGTH pin
   - PG_72_74 --> AUXOFF_PG pin

   If TPS259474x is selected, connect
   - OVLO_70_74 --> OVLO pin
   - PGTH_72_74 --> FLTB_PGTH pin
   - PG_72_74 --> AUXOFF_PG pin
8. Temperature dependent characteristics are not modelled.
   Thermal Shutdown Delay vs Power Dissipation is modelled such that temperature is not taken into account.
10. The simulation runs for 70m and takes approximately 10 minutes to run on a 4 core 2.8GHz machine.