As you said, I first remove the capacitor and TVS at the output end.
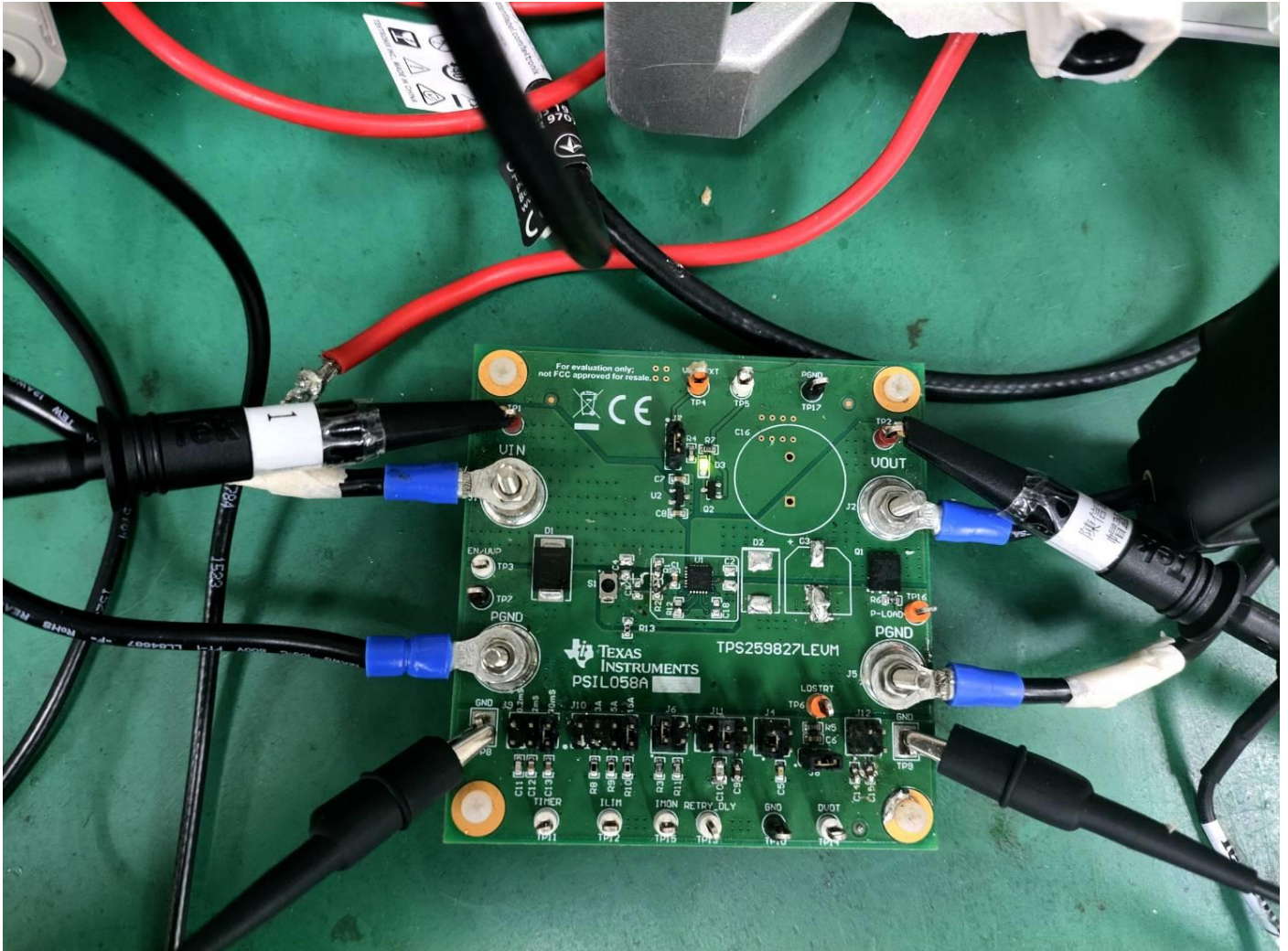
The picture below shows the current configuration.
dvdt sets Open
RETRY_DLY sets 1 s retry delay
ITIMER sets 20 ms delay
NRETRY (J4 Position) sets Infinite

The capacitor has been removed, which looks more consistent with Excel's calculation method.
After short circuit protection, it can also be successfully powered on with the load.

In Test items 5, it seems that the TSD protection is triggered, which means that if this test item is to be carried out in CR Mode and started with load when restarting after a short circuit, its limit may be around 6.7A.

The reason why Test items 5 failed seems to be that my voltage did not rise fast enough.
To trigger the protection function of TSD, is my understanding correct?

VIN (nom)	Nominal operating input voltage	20.00	V
VIN (max)	Maximum Operating input voltage (magnitude)	24.00	V
UVLOset	Undervoltage Threshold (VIN Rising)	16.00	V
V_{UVP}	Internal IN Undervoltage Protection Threshold (VIN Rising)	2.53	V
Cout	Load Capacitance	0.0	uF
Rlstart	Load at start-up (assumed to be resistive), Refer to Section 9.2.2.5.2 in Datasheet	3.0	Ohm
Imax	Maximum continuous load current (magnitude)	6.70	A

Calculations for SoftStart control (external cap on dVdt pin)				
Parameter	Description	Value	Units	Tolerance
Tchg_fastest	When no external capacitor is connected (max. slew rate)	2.72	ms	15.0%
Icharge_fastest	Charging current when charging at fastest possible rate If this current is < Ilimit, no capacitor is required at dVdT pin	0.00	A	
Tchg_req	The charging time required	2.73	ms	
Icharge_req	Charging (inrush) current desired in the system	3.00	A	
Cext_dvdt_cal1	Calculated value of capacitor at dVdT pin for required Tcharge	0.63	nF	
Cext_dvdt_cal2	Calculated value of capacitor at dVdT pin for required Icharge	0.00	nF	0.63
SELECT A CAPACITOR WITH THE CLOSEST POSSIBLE VALUE to max(Cext_dvdt_cal1, Cext_dvdt_cal2)				
CdVdT_ext	The external capacitor connecetd across dVdT pin	0.68	nF	10.0% 0.68
Icharge	Charging Current as per dVdT setting	0.00	A	18.0%
Does Device Enter Current Limit during start-up?		FALSE		#DIV/0!
Tchg_dVdT	Charging time set	2.72	ms	18.0%
Pd_Cout_startup	Power dissipation due to load cap at start-up	0.00	W	

Total Power dissipation at Start-up			
Pd_Rlstart	Power dissipation due to load resistance at start-up	22.22	W
Pd_startup	Total power dissipation at start-up	22.22	W
	Max power dissipation allowed for glitch-free startup for the programmed startup time (20% margin)	22.89	W 20.0% 28.61
	Will the system have glitch-free startup? Look at Thermal Shutdown Limit Plot Tab	YES	

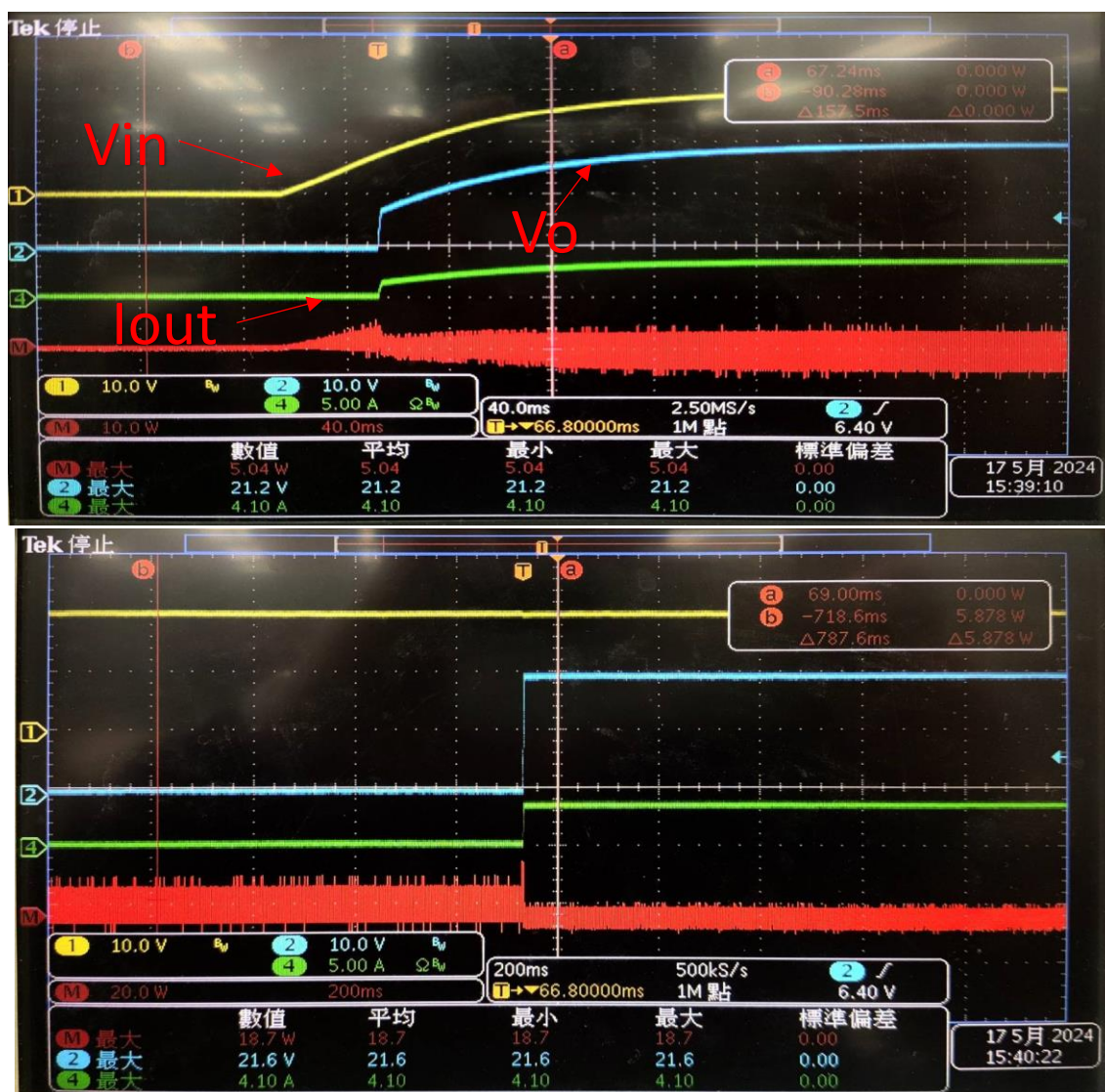Test items1.CR Mode R:6Ω(I=3.34A)，Vin 20V。 PASS

The picture below shows the current configuration.

The picture below shows the results of the test.

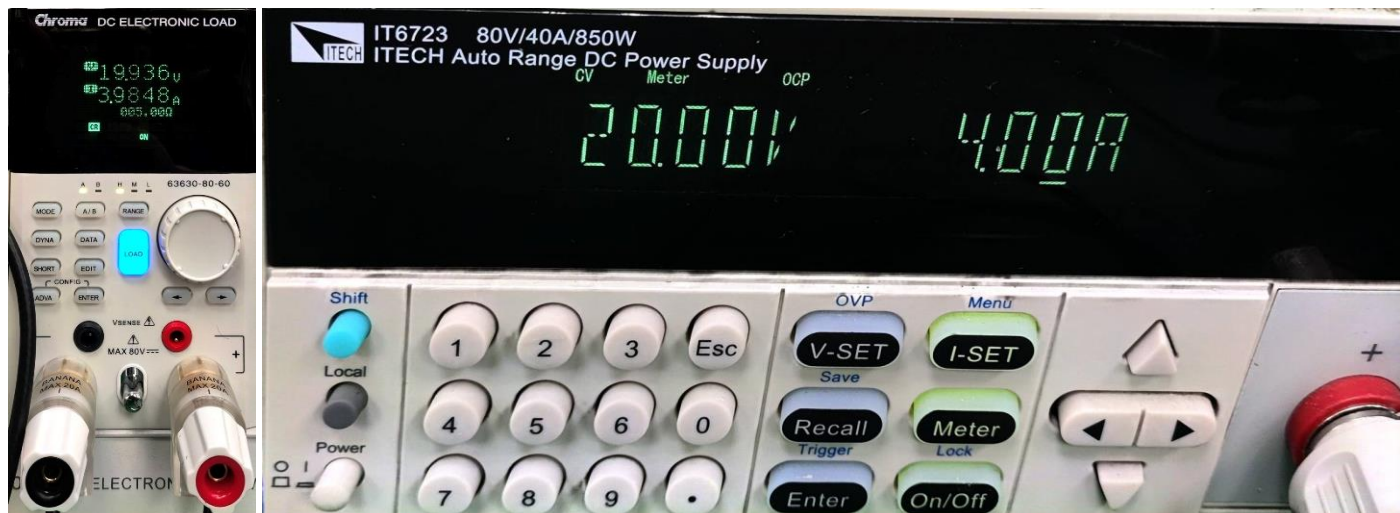The picture above shows: the status at startup.

The picture below shows: the state of restarting after circuit breaker protection.

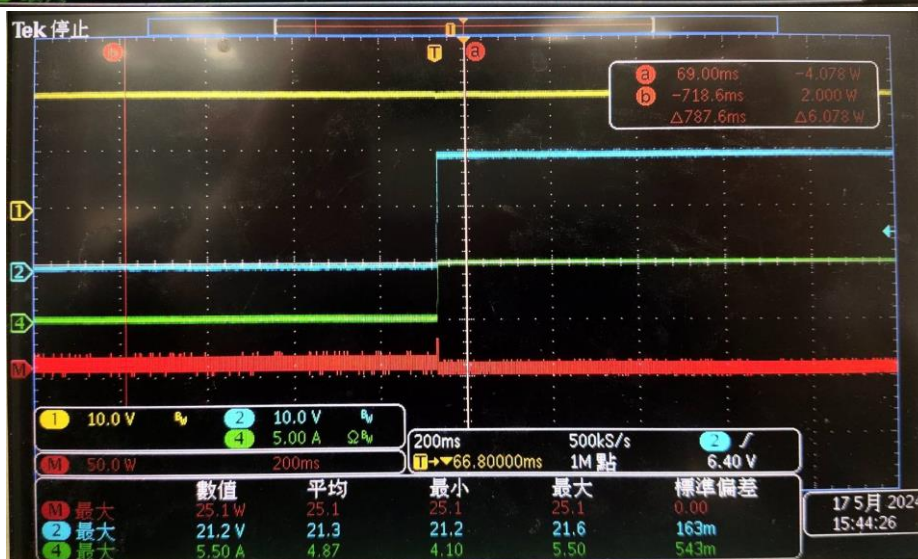Test items2.CR Mode R:5Ω(I=4A)，Vin 20V。PASS

The picture below shows the current configuration.

The picture below shows the results of the test.

The picture above shows: the status at startup.

The picture below shows: the state of restarting after circuit breaker protection.

Test items3.CR Mode R:4Ω(I=5A)，Vin 20V。 PASS

The picture below shows the current configuration。

The picture below shows the results of the test.

The picture above shows: the status at startup.

The picture below shows: the state of restarting after circuit breaker protection.

Test items4.CR Mode R:3Ω(I=6.6A)，Vin 20V。PASS

The picture below shows the current configuration.

The picture below shows the results of the test.

The picture above shows: the status at startup.

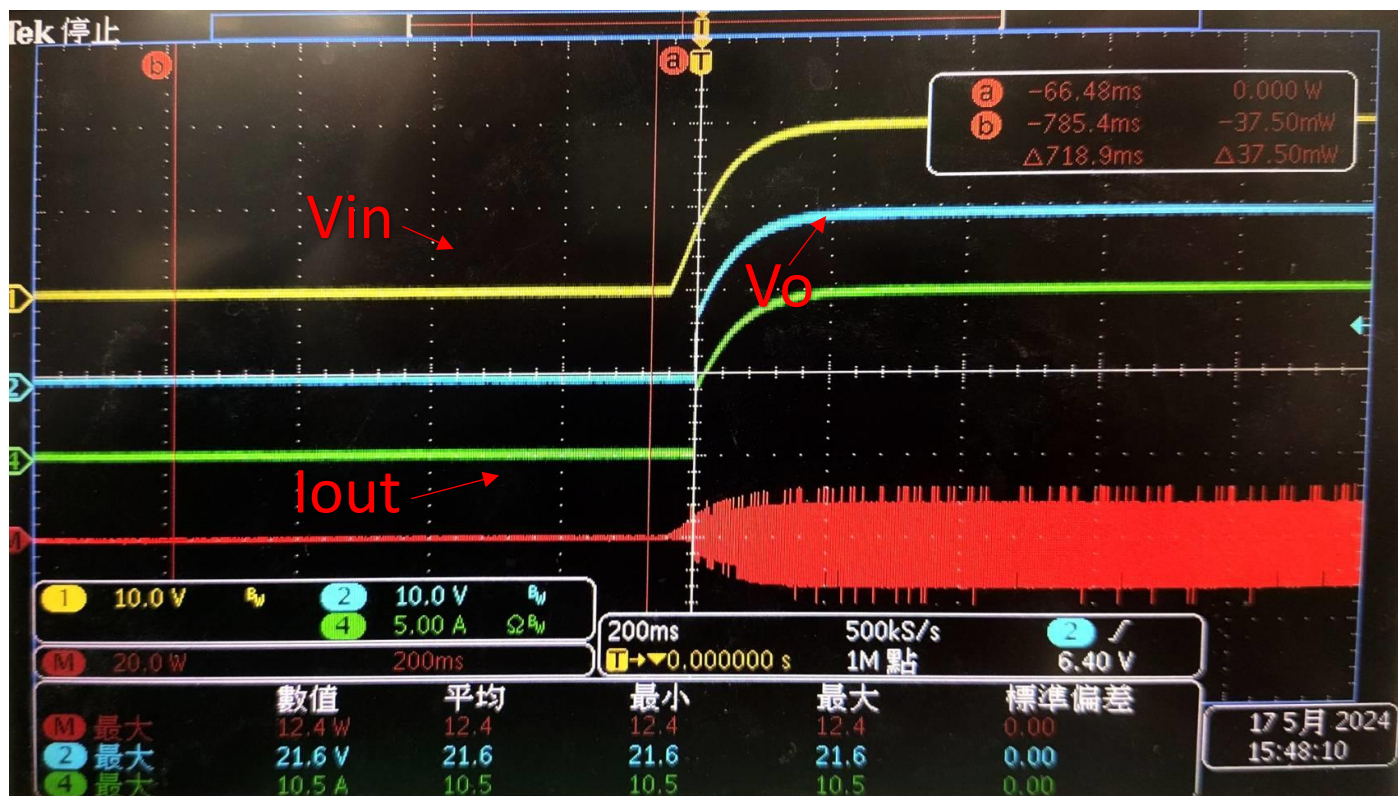The picture below shows: the state of restarting after circuit breaker protection.

Test items5.CR Mode R:2Ω(I=10A)，Vin 20V。 FAIL

The picture below shows the current configuration.
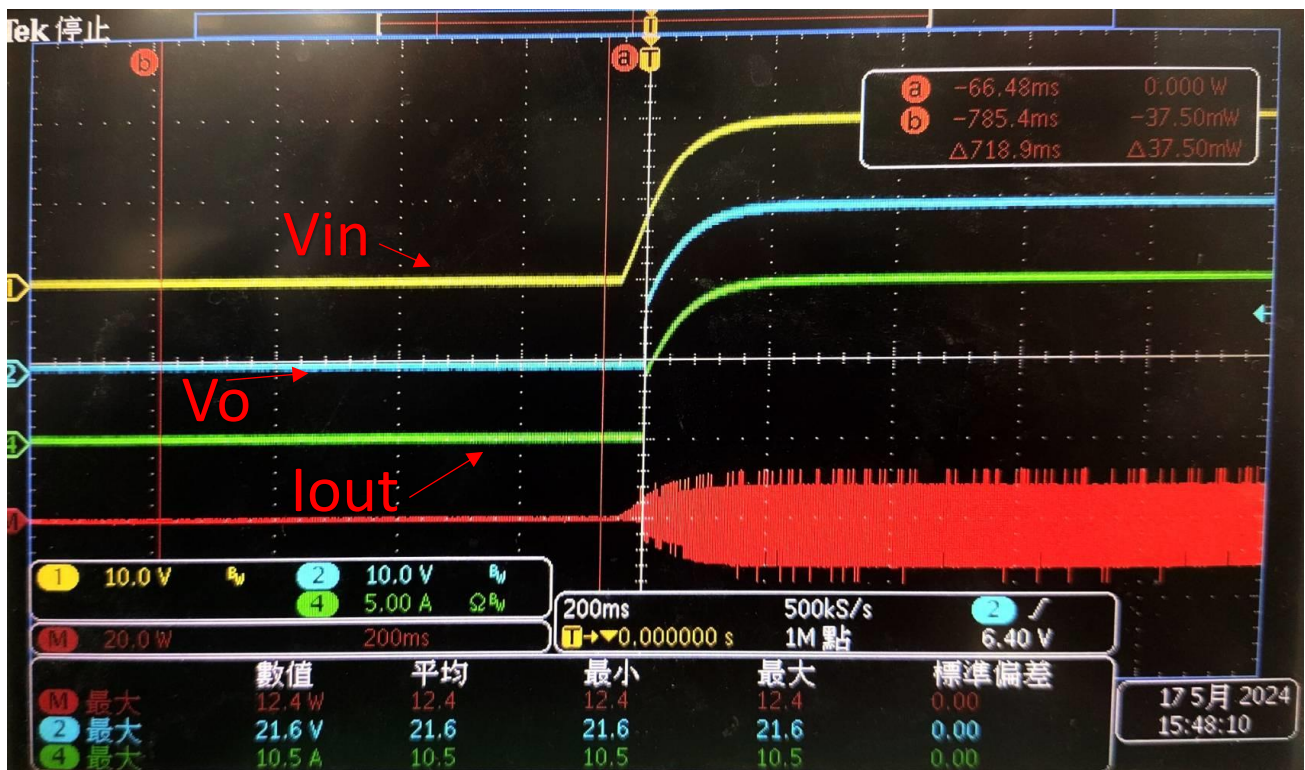

The picture below shows the results of the test.

The picture above shows: the status at startup. PASS

The picture above shows: the state of restarting after circuit breaker protection. FAIL

Auto-retry status

Waveform in Auto-retry state during Fail

Use the oscilloscope's cursor to capture the waveform.

At this time, Vin: 20V, VO rises to 17.2V, and current: 8A.

It seems that TSD protection is triggered.