TPS25984x, 4.5 - 16V, 0.8 mΩ, 50A Parallelizable eFuse with Accurate & Fast Current Monitor

1 Features

- Operating Voltage Range: 4.5 V to 16 V
  - 20 V Absolute Maximum
  - Withstands negative voltages up to -1 V at output
- Ultra-Low On-Resistance: R_{ON} = 0.8 mΩ (typ)
- Active High Enable Input with Adjustable Undervoltage Lockout (UVLO)
- Fast Overvoltage Protection (fixed 16.7 V)
- Adjustable Output Slew Rate Control (dVdt) for inrush current protection
- Precise load current monitoring
  - <3 % error over 50-100% of max current
  - 1 MHz bandwidth
- Robust Overcurrent protection
  – Circuit-breaker response
  – Adjustable Threshold: 10 A to 60 A
  – Overcurrent Protection Threshold Accuracy: ±5% (max)
  – Adjustable transient overcurrent timer to support peak currents up to 60 A for TBD ms
  – Fast trip response (<200 ns) to short-circuit events
    - Adjustable threshold
    - Immune to supply line transients
- Supports parallel connection of multiple eFuses with device state synchronization and equal load sharing during start-up and steady state
- Overtemperature Protection (OTP) with analog die temperature monitor output (TEMP)
- FET health monitoring and reporting
- Fault Indication Pin ($\overline{FLT}$)
- Power Good Indication Pin (PG)
- Small Footprint: QFN-32 5mmx5mm, 0.5mm pitch

2 Applications

- Server Motherboard/Add-on cards
- Graphics/Accelerator cards
- Switches/Routers
- Fan trays

3 Description

The TPS25984x is an integrated high current circuit protection and power management solution in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short circuits and excessive inrush current. Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit level can be set by user as per system needs. A user adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse.
An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management such as Intel PSYS and PROCHOT to optimize server and data-center performance. Multiple eFuses can be connected in parallel to increase the total current capacity for high power systems. All devices share current equally during start-up as well as steady state to avoid overstressing some of the devices resulting in premature or partial shutdown of the parallel chain.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TPS25984xRZJ	QFN (32)	5 mm x 5 mm

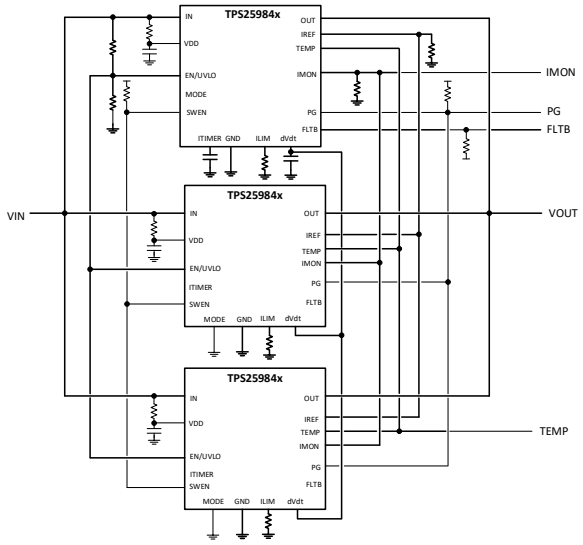

Figure 1 - Simplified Schematics – Parallel Operation

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4 Device Comparison Table

Part Number	Response to Fault
TPS259840RZJR	Latch-Off
TPS259841RZJR	Auto-Retry

5 Terminal Configuration

TPS25984x RZJ Package
32-pin QFN

Top View

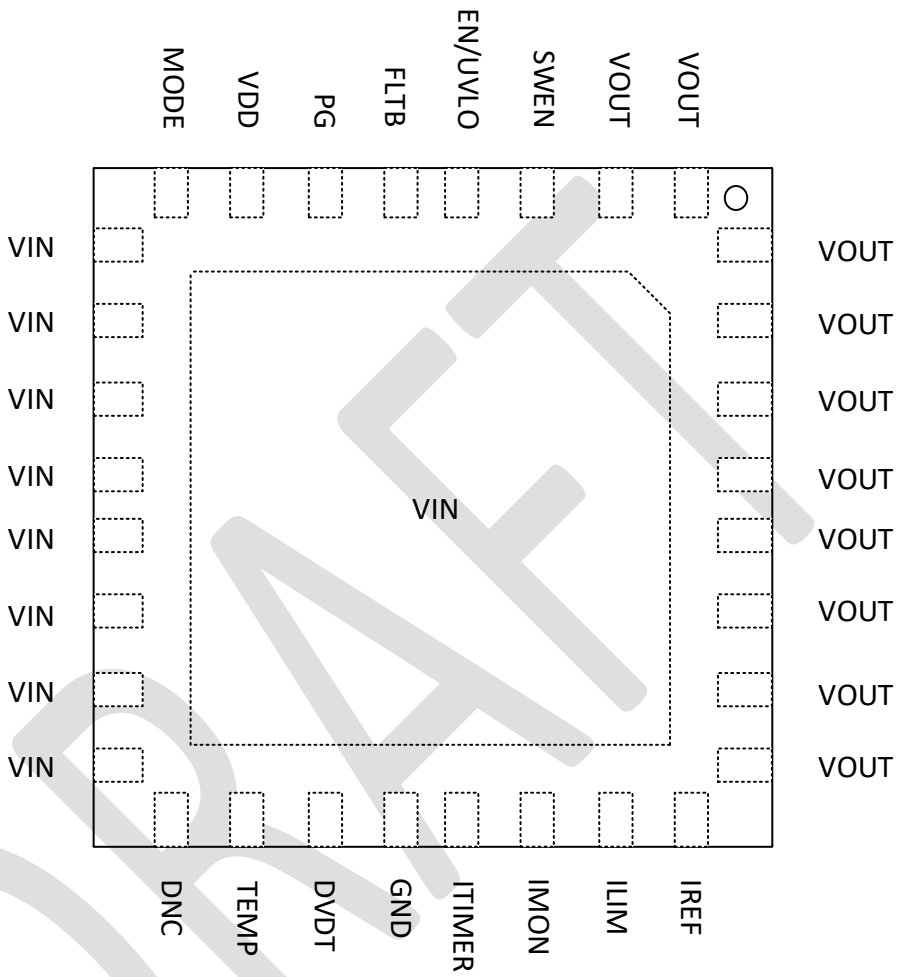


Figure 2 - Pinout

Pin #	Pin Name	Pin Type	Description
1,2, 25-32	OUT	Power/Thermal	Power Output. Must be soldered to output power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
3	SWEN	Digital Input/Output	Open drain signal to indicate and control power switch ON/OFF status. This facilitates synchronization of multiple devices in a parallel chain.
4	EN/UVLO	Analog Input	Active High Enable input. Connect resistor divider from input supply to set the Undervoltage threshold. **Do not leave floating.**
5	FLTB	Digital Output	Open Drain Active Low FAULT output.
6	PG	Digital Input/Output	Open Drain Active High PGOOD output.
7	VDD	Power	Controller power input pin. Can be used to power the internal control circuitry with a filtered/stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.

8	MODE	Analog Input	Pin to configure the device for standalone/primary or secondary mode. Connect the pin to GND to configure device as a secondary to a primary eFuse/controller. Leave the pin floating for standalone/primary mode of operation.
9-16, EXP PAD	IN	Power/Thermal	Power Input. Must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
17	DNC	N/A	Internal test mode pin. **Do not connect externally.**
18	TEMP	Analog Output	Die (Controller) Temperature Monitor. Analog Voltage output. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to get the peak temperature of the chain.
19	DVDT	Analog Input/Output	Startup Output Slew Rate control pin. Leave it open to allow fastest startup. Connect capacitor to ground to slow down the slew rate to manage inrush current.
20	GND	Ground	Device Ground reference pin. Connect to System Ground.
21	ITIMER	Analog Input/Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed the circuit-breaker threshold (but lower than fast-trip threshold) in steady state before the device overcurrent response takes action.
22	IMON	Analog Output	An external resistor from this pin to GND sets the overcurrent/circuit-breaker threshold and fast trip threshold during steady state. This pin also acts as a fast and accurate analog output load current monitor signal during state. **Do not leave floating.**
23	ILIM	Analog Output	An external resistor from this pin to GND sets the current limit threshold and fast trip threshold during start-up. This also sets the active sharing threshold during steady state. **Do not leave floating.**
24	IREF	Analog Input/Output	Reference voltage for overcurrent protection and active current sharing blocks. Can be generated using internal current source and resistor on this pin (standalone configuration), or can be driven externally (primary/secondary configuration). **Do not leave floating.**

6 Specifications

6.1 Absolute Maximum Ratings(1)

Parameter	Description	Pin	Min	Max	Units
V_{INMAX}	Maximum Input Voltage Range	IN	–0.3	20	V
$V_{INMAX,PLS}$	Maximum Input Voltage Range (100 µs, $T_A \geq 0$ °C)	IN	–0.3	TBD	V
V_{DDMAX}	Maximum Supply Voltage Range	VDD	–0.3	20	V
V_{OUTMAX}	Maximum Output Voltage Range	OUT	–1	Min(20 V, VIN + 0.3)	V
$V_{OUTMAX,PLS}$	Maximum Output Voltage Range (100 µs, $T_A \geq 0$ °C)	OUT	–1	Min(TBD V, VIN + 0.3)	V
$V_{IREFMAX}$	Maximum IREF Pin Voltage Range	IREF		5.5	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage Range	DVDT		5.5	V
$V_{MODEMAX}$	Maximum MODE Pin Range	MODE		5.5	V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage Range	SWEN		5.5	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink Current	SWEN		10	mA
V_{ENMAX}	Maximum Enable Pin Voltage Range	EN/UVLO		20	V
$V_{FLTBMAX}$	Maximum FLT Pin Voltage Range	FLT		5.5	V
$I_{FLTBMAX}$	Maximum FLT Pin Sink Current	FLT		10	mA
V_{PGMAX}	Maximum PG Pin Voltage Range	PG		5.5	V
I_{PGMAX}	Maximum PG Pin Sink Current	PG		10	mA
V_{TEMP}	Maximum TEMP Pin Voltage Range	TEMP		TBD	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Soldering Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) See TSD specification in *Electrical Characteristics* section and *Thermal Considerations* section.

6.2 ESD Ratings

				VALUE	UNIT
ESD	Electrostatic discharge protection	Human-Body Model (HBM)(1)	All pins	±2000	V
		Charged-Device Model (CDM)(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process..
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Parameter	Description	Pin	Min	Max	Units
V_{IN}	Input Voltage Range	IN	4.5	16	V
V_{DD}	Supply Voltage Range	VDD	4.5	16	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5	V
V_{dVdT}	dVdT Pin Cap Voltage Rating	dVdT	4		V
V_{PG}	PG Pin Pull-up Voltage Range	PG		5	V
V_{FLTB}	FLT Pin Pull-up Voltage Range	FLT		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN		5	V
V_{ITIMER}	ITIMER Pin Cap Voltage Rating	ITIMER	4		V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
I_{MAX}	Continuous Switch Current	IN to OUT		50	A
$I_{MAX, PLS}$	Peak Output Current (2ms) with TBD duty cycle, $T_J \leq 125$ °C	IN to OUT		70	A
T_A	Ambient temperature		–40	85	°C
T_J	Junction temperature		–40	125	°C

6.4 Thermal Information

Thermal Parameters (1)(2)		TPS25984x	Unit
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	N/A	
θ_{JB}	Junction-to-board thermal resistance	N/A	
Ψ_{JT}	Junction-to-top characterization parameter	TBD	
Ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) Based on simulations conducted with the device mounted on a custom 8-layer 3” x 4”n PCB (4s4p) with 2 oz top and bottom layer and TBD vias each under IN and OUT.

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) V_{IN} = V_{DD} = 12 V, –40°C ≤ T_J ≤ +125 °C, $V_{EN/UVLO}$ = 2 V, R_{ILIM} = TBD Ω, C_{dVdT} = OPEN, OUT = Open, ITIMER = Open. Typical values are for operation at 25°C. All voltages referenced to GND.

Parameter	Description	Tet condition	Min	Typ	Max	Units
INPUT SUPPLY (VDD)						
V_{DD}	Input voltage range		4.5		16	V
$I_{QON(VDD)}$	VDD ON state quiescent current	$V_{VDD} > V_{UVP(R)}$, $V_{EN} \geq V_{UVLO(R)}$		2		mA
$I_{QOFF(VDD)}$	VDD OFF state current	$V_{SD(R)} < V_{EN} < V_{UVLO}$				uA
$I_{SD(VDD)}$	VDD shutdown current	$V_{EN} < V_{SD(F)}$				uA
$V_{UVP(R)}$	VDD Undervoltage Protection Threshold	VDD Rising	4	4.3	4.5	V
$V_{UVP(F)}$	VDD Undervoltage Protection Threshold	VDD Falling	3.9	4.2	4.4	V
$V_{UVP(HYS)}$	UVP Hysteresis VDD					mV
INPUT SUPPLY (VDD)						
V_{IN}	Input voltage range		4.5		16	V
$V_{UVPIN(R)}$	VIN Undervoltage Protection Threshold	VIN Rising	4	4.3	4.5	V
$V_{UVPIN(F)}$	VIN Undervoltage Protection Threshold	VIN Falling	3.9	4.2	4.4	V
$I_{QON(IN)}$	IN ON state quiescent current	$V_{EN} \geq V_{UVLO(R)}$		2		mA
$I_{QOFF(IN)}$	IN OFF state current	$V_{SD(R)} < V_{EN} < V_{UVLO}$				uA
$I_{SD(IN)}$	IN shutdown current	$V_{EN} < V_{SD(F)}$				uA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO pin voltage threshold for turning on, rising	EN/UVLO Rising		1.2		V
$V_{UVLO(F)}$	EN/UVLO pin voltage threshold for turning off and engaging QOD, falling	EN/UVLO Falling		1.1		V
$V_{UVLO(HYS)}$	UVLO Hysteresis			100		mV
$V_{SD(F)}$	Shutdown threshold	EN/UVLO Falling	0.6	0.8		V
$V_{SD(R)}$	Shutdown threshold	EN/UVLO Rising		0.8		V
I_{ENLKG}	EN/UVLO pin leakage current				0.1	uA
OVERVOLTAGE LOCKOUT (IN)						
$V_{OVP(R)}$	Overvoltage protection threshold (rising)	VIN rising		16.7		V
$V_{OVP(F)}$	Overvoltage protection threshold (falling)	VIN falling		16.6		V
$V_{OVP(HYS)}$	Overvoltage protection threshold (Hysterisis)			100		mV
ON-RESISTANCE (R_{ON}) – IN to OUT						
R_{ON}	ON state resistance	I_{OUT} = TBD A, T_J = 25 °C		0.8		mΩ
		I_{OUT} = TBD A, T_J = -40 to 125 °C			1.2	mΩ
CURRENT LIMIT REFERENCE (IREF)						
V_{IREF}	IREF pin recommended voltage range		0.3		1.2	V
I_{REFLkg}	Leakage at 1.2V			TBD		
I_{IREF}	IREF internal sourcing current		24.5	25	25.5	uA
OUTPUT CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	Current Monitor Gain (ILIM:IOUT) vs. IOUT.	Device in steady state (PG asserted)	48.95	50	51.05	uA/A
$I_{LKG(ILIM)}$	ILIM leakage/offset current					uA
$CL_{REF(SAT)}$	Ratio of Inrush current limit to steady state circuit-breaker threshold	$V_{OUT} > V_{FB}$, PG not asserted		70		%
I_{HOLD}	IOUT Start-up Current limit regulation threshold	R_{ILIM} = TBD Ω, V_{IREF} = TBD V, $V_{OUT} > V_{FB}$		40.6		A
		R_{ILIM} = TBD Ω, V_{IREF} = TBD V, $V_{OUT} > V_{FB}$	32.5	35	37.5	A
		R_{ILIM} = TBD Ω, V_{IREF} = TBD V,		14		A

		$V_{OUT} > V_{FB}$				
		R_{ILIM} = TBD Ω, V_{IREF} = TBD V, $V_{OUT} > V_{FB}$		7		A
I_{FB}	Foldback current	R_{IMON} = TBD Ω, V_{IREF} = TBD V, V_{OUT} = 0V		TBD		A
		R_{IMON} = TBD Ω, V_{IREF} = TBD V, V_{OUT} = 0V		TBD		A
		R_{IMON} = TBD Ω, V_{IREF} = TBD V, V_{OUT} = 0V		TBD		A
V_{FB}	Foldback voltage			2.0		V
OUTPUT CURRENT MONITOR (IMON)						
G_{IMON}	Current Monitor Gain (IMON:IOUT)	Device in steady state (PG asserted)	48.95	50	51.05	uA/A
$I_{LKG(IMON)}$	IMON leakage/offset current vs. VIN					uA
I_{OCP}	IOUT Current limit OCP (Circuit-Breaker) threshold	R_{IMON} = TBD Ω, V_{IREF} = TBD V	56	58	60	A
		R_{IMON} = TBD Ω, V_{IREF} = TBD V	48.3	50	51.7	A
		R_{IMON} = TBD Ω, V_{IREF} = TBD V	24.1	25	25.9	A
		R_{IMON} = TBD Ω, V_{IREF} = TBD V	11.5	12	12.5	A
OVERCURRENT FAULT BLANKING TIMER (ITIMER)						
R_{ITMR}	ITIMER pin internal pull-up resistance			15		kΩ
I_{ITMR}	ITIMER pin internal discharge current	$I_{OUT} > I_{OCP}$, ITIMER ↓		2		uA
V_{ITMR}	ITIMER pin internal pull-up voltage	$I_{OUT} < I_{OCP}$		2.5		V
$V_{ITMRTHR}$	ITIMER comparator falling threshold	$I_{OUT} > I_{LIM}$, ITIMER ↓		1		V
ΔV_{ITMR}	ITIMER discharge voltage	$I_{OUT} > I_{OCP}$, ITIMER ↓		1.5		V
Fixed Fast-trip (IN-OUT)						
V_{DSCOMP}	VDS comparator fixed fast trip threshold in steady state	PG asserted High, MODE = Open		85		mV
		PG asserted High, MODE = GND		125		mV
Scalable Fast-trip						
$SFT_{REF(LIN)}$	Scalable fast trip threshold to circuit breaker threshold ratio (Steady state)	Standalone/Primary mode (MODE = Open)		200		%
$SFT_{REF(SAT)}$	Scalable fast trip threshold to circuit breaker threshold ratio (Inrush)	Standalone/Primary mode (MODE = Open)		150		%
$SFT_{REF(LIN)}$	Scalable fast trip threshold to circuit breaker threshold ratio (Steady state)	Minion mode (MODE = GND)		210		%
$SFT_{REF(SAT)}$	Scalable fast trip threshold to circuit breaker threshold ratio (Inrush)	Minion mode (MODE = GND)		150		%
Active current sharing						
$R_{ON(ACS)}$	Maximum RON during Active current sharing	$V_{ILIM} > 1.1 \times (1/3) \times V_{IREF}$		TBD		mΩ
$G_{IMON(ACS)}$	IMON:IOUT ratio during active current limiting	PG asserted High, $V_{ILIM} > 1.1 \times V_{IREF}$		TBD		uA/A
$CL_{REF(ACS)}$	Ratio of Active current sharing trigger threshold to steady state circuit-breaker threshold	PG asserted High		110		%
OUTPUT SLEW RATE CONTROL (dV/dt)						
I_{DVDT}	dVdt Pin Charging Current (Primary/Standalone mode)	MODE = Open		2		uA
G_{DVDT}	dVdt Gain			20		V/V
$I_{DVDTLKG}$	dVdt Pin Leakage Current (Secondary mode)	MODE = GND		10		nA
R_{DVDT}	dVdt Pin to GND Discharge Resistance			10		Ω
Quick Output Discharge (OUT)						
R_{QOD}	Quick Output Discharge pull-down resistance	$V_{SD(R)} < V_{EN} < V_{UVLO}$		500		Ω
Temperature Monitor (TEMP)						

G_{TMP}	TEMP sensor gain			TBD		mV/℃
V_{TMP}	TEMP pin output voltage	T_J = 25 ℃		500		mV
I_{TMPSRC}	TEMP pin sourcing current			15		uA
I_{TMPSNK}	TEMP pin sinking current			1		uA
Overtemperature Protection (OTP)						
TSD	Absolute Thermal Shutdown Rising Threshold	T_J Rising		150		°C
TSD_{HYS}	Absolute Thermal shutdown hysteresis	T_J Falling		10		°C
AutoRetry	Auto-Retry vs Latch-off function	TPS259840		Latch-off		
		TPS259841		Auto-Retry		
FET Health Monitoring						
V_{DSFLT}	FET D-S Fault Threshold	SWEN = L		0.5		V
V_{DSOK}	FET D-S Fault Recovery Threshold	SWEN = L		0.6		V
V_{GDFLT}	FET G-S Threshold to detect G-D Fault	SWEN = H		2		V
V_{GSFLT}	FET G-S Threshold to detect G-S Fault	SWEN = H		1		V
Single Point Failure (ILIM, IMON, IREF)						
$I_{OC\_BKP(LIN)}$	Back-up overcurrent protection threshold (Steady steady)		65	90		A
$I_{OC\_BKP(SAT)}$	Back-up overcurrent protection threshold (Inrush)		55	76		A

6.6 Timing Requirements

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	V_{IN} > V_{OVP} V to SWEN↓		1.5		us
t_{Insdly}	Insertion delay	V_{DD} > $V_{UVP(R)}$ to SWEN↑		10		ms
t_{FFT}	Fixed Fast-Trip response time Hard Short	V_{DS} > 1.3 x V_{DSCOMP} to I_{OUT}↓		200		ns
t_{SFT}	Scalable Fast-Trip response time	I_{OUT} > 3 x I_{OCP} to IOUT↓		400		ns
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.3 x I_{OCP}, C_{ITIMER} = Open		0		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.3 x I_{OCP}, C_{ITIMER} = 4.7nF		2		ms
t_{ITIMER}	Overcurrent blanking interval	I_{OUT} = 1.3 x I_{OCP}, C_{ITIMER} = Short to GND		0		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant, Primary mode (MODE = Open)		100		ms
t_{REC}	Fault Recovery Time	Secondary mode (MODE = GND), SWEN↓ to SWEN↑		10		us
$t_{EN(DG)}$	EN/UVLO de-glitch time		1			us
$t_{SWEN(FLT)}$	Primary device fault detection de-glitch time	MODE = GND, SWEN_INT↑ to SWEN↓		10		us
$t_{SWEN(DG)}$	SWEN de-glitch time (steady state)		1			us
$t_{SWEN(D)}$	SWEN de-assertion delay				5	us
$t_{SWEN(TO)}$	SWEN low interval to disable fast recovery		100			us
t_{SPFAIL_TMR}	Single point failure backup timer interval	I_{OUT} = 1.3 x I_{REF}, ITIMER forced to 2 V		50		ms
t_{GSFLT}	G-S Fault timer interval in steady state	INRUSH DONE, SWEN = H, V_{GS} < V_{GSFLT} to FLT↓		10		us
t_{DSFLT}	D-S Fault timer interval			800		ms
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		200		ms
t_{FLTB}	FLT assertion delay			1		us
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}, C_{OUT} = 1mF		2.5		s
t_{QOD}	QOD enable timer	V_{SD} < $V_{EN/UVLO}$ < V_{UVLO}	1			ms
t_{PGA}	PG assertion delay			10		us
t_{PGDO}	PG De-assertion de-glitch	Primary mode MODE = Open		10		µs
t_{PGDI}	PG Detection de-glitch	Secondary mode MODE = GND, PG↓ to ??	1			µs

6.7 Switching Characteristics:

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See *Slew Rate and Inrush Current Control (dVdt)* section for more details.

The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_L) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical Values are taken at T_J = 25°C unless specifically noted otherwise.

Typical Values taken at T_J = 25 °C. R_{OUT} = 100 Ω, C_{OUT} = 1 mF

SYMBOL	PARAMETER	C_{dVdt} (pF)		UNIT
		Open	3300	
SR_{ON}	Rising Slew Rate	TBD	TBD	mV/ us
$t_{D,ON}$	Turn-On Delay	TBD	TBD	us
t_R	Rise Time	TBD	TBD	us
t_{ON}	Turn-On Time	TBD	TBD	us
$t_{D,OFF}$	Turn-Off Delay	TBD	TBD	us
t_F	Fall Time	Depends on R_L and C_L		us

Table 1 – Typical Switching Characteristics

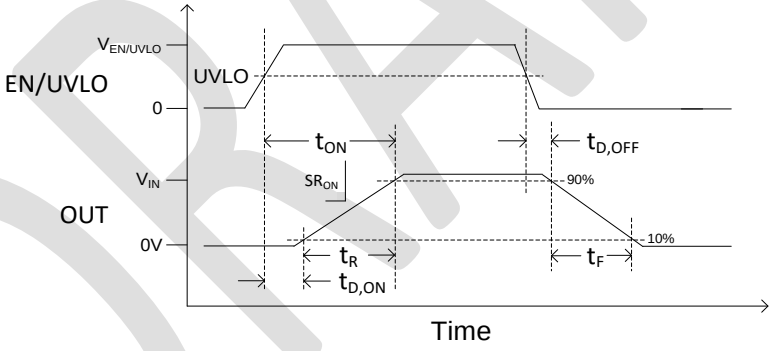


Figure 3 – TPS25984x Switching Times

7 Detailed Description

7.1 Overview

The TPS25984x is an eFuse with integrated power switch that is used to manage load voltage and load current. The device starts its operation by monitoring the VDD and IN bus. When V_{DD} & V_{IN} exceed the respective Undervoltage Protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next, it samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low, the internal MOSFET is turned off.

After a successful start-up sequence, the TPS25984x device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the programmed overload current limit I_{LIM} is not exceeded and overvoltage spikes on V_{IN} are cut-off. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This facilitates the implementation of advanced dynamic platform power management techniques to maximize system power utilization and throughput without sacrificing safety and reliability.

For systems needing higher load current support, multiple TPS25984x eFuses can be connected in parallel. All devices share current equally during start-up as well as steady state to avoid overstressing some of the devices more than others resulting in pre-mature or partial shutdown of the parallel chain. The devices synchronize their operating states to ensure graceful startup, shutdown and response to faults.

The device has integrated protection circuits to ensure device safety and reliability under recommended operating conditions. The internal FET is protected at all time using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (Tj) becomes too hot.

7.2 Functional Block Diagram

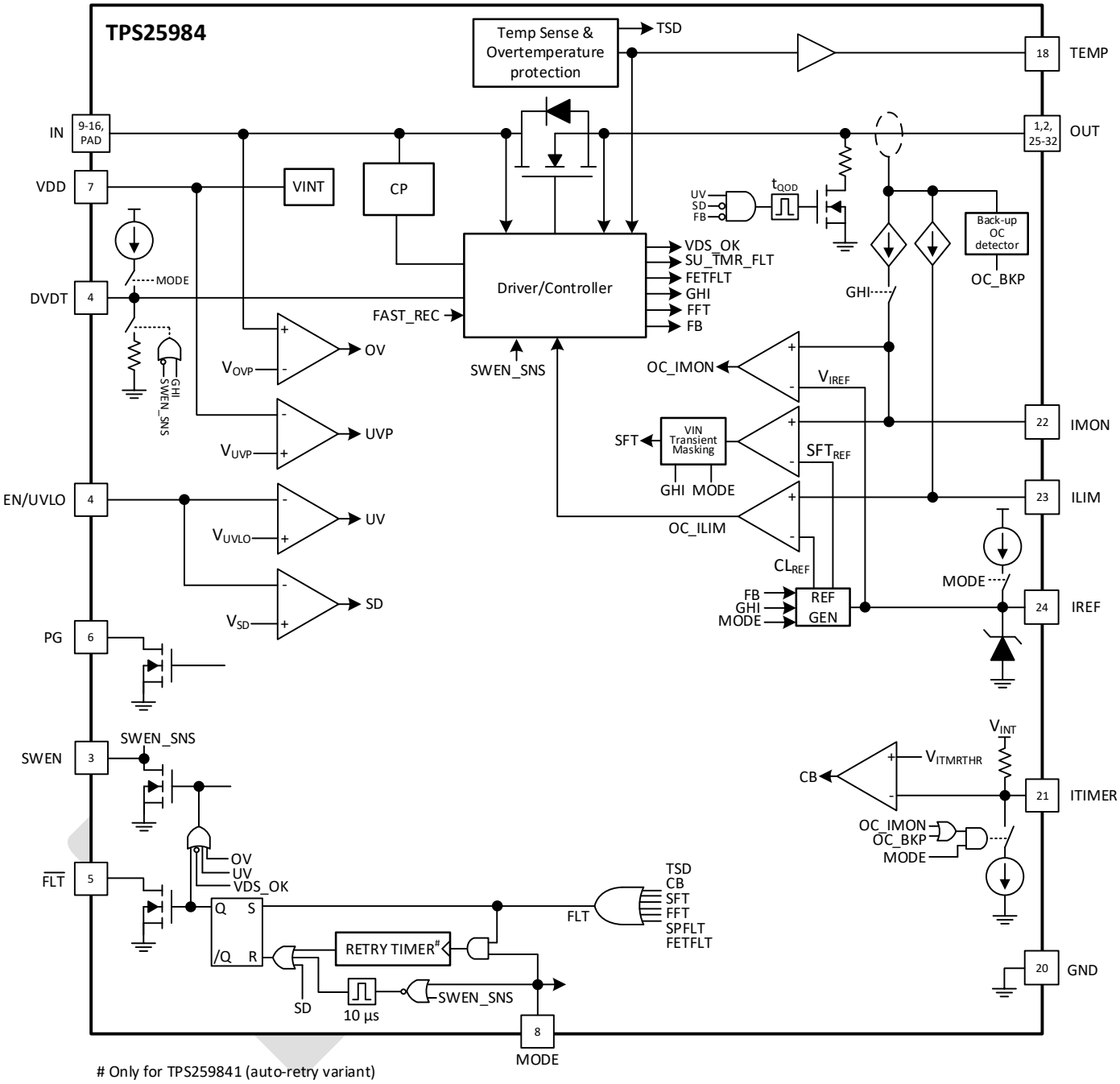


Figure 4 – TPS25984x Block Diagram

7.3 Feature Description

The TPS25984x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO & UVP)

The TPS25984x implements Undervoltage Lockout on VDD & VIN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage lockout has a default lockout threshold of V_{UVP} internally on VDD and V_{UVPIN} on V_{IN}. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The figure and equation below shows how a resistor divider can be used to set the UVLO set point for a given voltage supply.

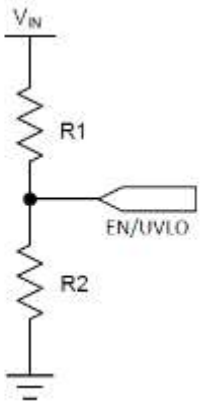


Figure 12 – Programmable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R1 + R2)}{R2}$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO}$: Device is fully ON
2. $V_{SD} < V_{EN} < V_{UVLO}$: The FET along with most of controller circuit is turned OFF, except some critical bias and digital circuitry. Holding EN/UVLO pin in this state for >1 ms activates the Output Discharge function.
3. $V_{EN} < V_{SD}$: All active circuitry inside the part is turned OFF and it retains no digital state memory. In this condition, the device quiescent current consumption is at a minimum.

7.3.1.1 Insertion delay

The TPS25984x implements insertion delay at start-up to ensure the supply has stabilized before the device tries to turn on. This is to prevent any unexpected behavior in the system if the device tries to turn on while the card has not made firm contact with the backplane or if there's any supply ringing/oscillation during startup.
The device initially waits for the VDD supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, it remains off for an additional delay of 10 ms irrespective of the EN/UVLO pin condition.

7.3.2 Overvoltage Protection (OVP)

The TPS25984x implements Overvoltage Lockout to protect the load from input overvoltage conditions. The OVP comparator on the IN pin uses a fixed internal Overvoltage Protection threshold equal to V_{OVP}.

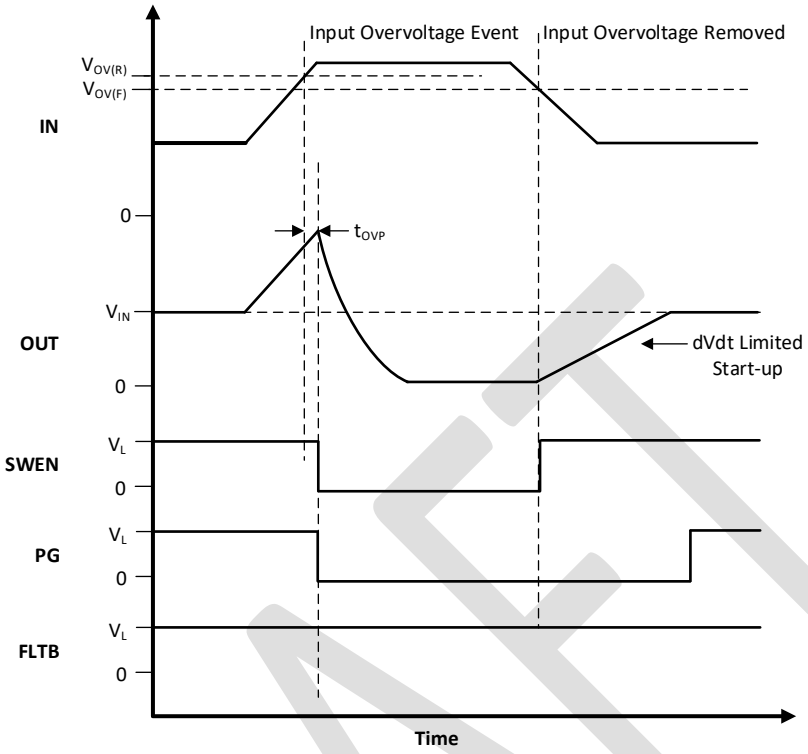


Figure 11 – TPS25984x Overvoltage Protection Response

7.3.3 Inrush Current, Overcurrent, and Short Circuit Protection

TPS25984x incorporates three levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Active current limit with adjustable threshold (I_{LIM}) for overcurrent protection during start-up
3. Circuit breaker with adjustable threshold (I_{OCP}) and blanking timer (ITIMER) for overcurrent protection during steady state
4. Fast-trip response to severe overcurrent faults with adjustable threshold (I_{SFT}) to quickly protect against hard short-circuits under all conditions, and fixed threshold (I_{FFT}) during steady state.

7.3.3.1 Slew Rate and Inrush Current Control (dVdt)

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. The following equation can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_L):

$$SR\,(mV/\mu s) = \frac{I_{INRUSH}(mA)}{C_L\,(\mu F)}$$

A capacitance can be added to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the following formula:

$$C_{DVDT}\,(pF) = \frac{42000}{SR\,(mV/\mu s)}$$

This is also a function of the energy dissipated during start-up.

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note: High input Slew Rates in combination with high input inductance may result in oscillations during startup. This can be mitigated using one or more of the following steps:

1. Reducing the input inductance
2. Increasing the capacitance on VIN pin
3. Increasing the dVdt pin capacitance to reduce the slew rate

NOTE: It's recommended to have a minimum start-up time of 5ms to prevent oscillations during start-up.

7.3.3.1.1 Active Current Balancing during inrush

The TPS25984x implements a proprietary current balancing mechanism during inrush, which allows multiple eFuses connected in parallel to share current nearly equally. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance helps to support larger load capacitors on high current platforms without compromising on the inrush time or system reliability.

7.3.3.1.2 Start-up timeout

If the start-up (i.e. GHI assertion) is not completed within a timeout interval (TBD ms) after SWEN_SNS is asserted, the device registers it as a fault. FLTB is asserted low and the device goes into latch-off/auto-retry mode depending on the configuration.

7.3.3.2 Circuit Breaker (I_{OCP})

The TPS25984x responds to output overcurrent conditions during steady state by turning off the output after a user adjustable transient fault blanking interval. The device constantly senses the output load current and provides an analog current output on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}).

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON}$$

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a threshold. The reference voltage (V_{IREF}) can be generated in 2 ways, which changes the overcurrent detection threshold (I_{LIM} or I_{OCP}) accordingly:

1. In standalone mode of operation, the internal current source interacts with the external IREF pin resistor to generate the reference voltage.

$$V_{IREF} = I_{IREF} \times R_{IREF}$$

2. In a primary secondary configuration, the primary eFuse/controller drives the voltage on IREF pin to provide an external reference (V_{IREF}).

   The circuit-breaker threshold during steady state (I_{OCP}) can be calculated as:

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}}$$

Note: Ensure to maintain V_{IREF} below the recommended voltage to ensure proper operation of overcurrent detection circuit.

Once a overcurrent condition is detected i.e. the load current exceeds the programmed current limit threshold (I_{OCP}), but lower than the short circuit threshold (2 x I_{OCP}), the device starts discharging the ITIMER pin capacitor using an internal TBD-µA pull down current. If the load current drops below the current limit threshold before the ITIMER capacitor discharges to V_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit breaker action is not engaged. This allows short load transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor continues to discharge and once it falls below V_{ITIMER}, the circuit breaker action turns off the FET immediately. At the same time, the ITIMER cap is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. The following equation can be used to calculate the R_{ILIM} value for a desired current limit.

NOTE:

1. Leaving the IMON pin Open sets the current limit to nearly zero and results in the part breaking the circuit with the slightest amount of loading at the output.
2. Shorting the IMON pin to ground at any point during normal operation is detected as a fault and the part shuts down using the mechanism described in the ***IMON pin single point failure*** section. There's a minimum current (I_{OC_BKP}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculation using the equation below.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)}$$

NOTE:

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the Iq – Not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval, but it also extends the time needed for the ITIMER cap to recharge up to VINT before the next overcurrent event. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it will take lesser time to discharge to the VITIMER threshold, thereby providing a shorter blanking interval than intended.

Once the part shuts down due to a Circuit Breaker fault, it would either stay latched off (TPS259840 variant) or restart automatically after a fixed delay (TPS259841 variant).

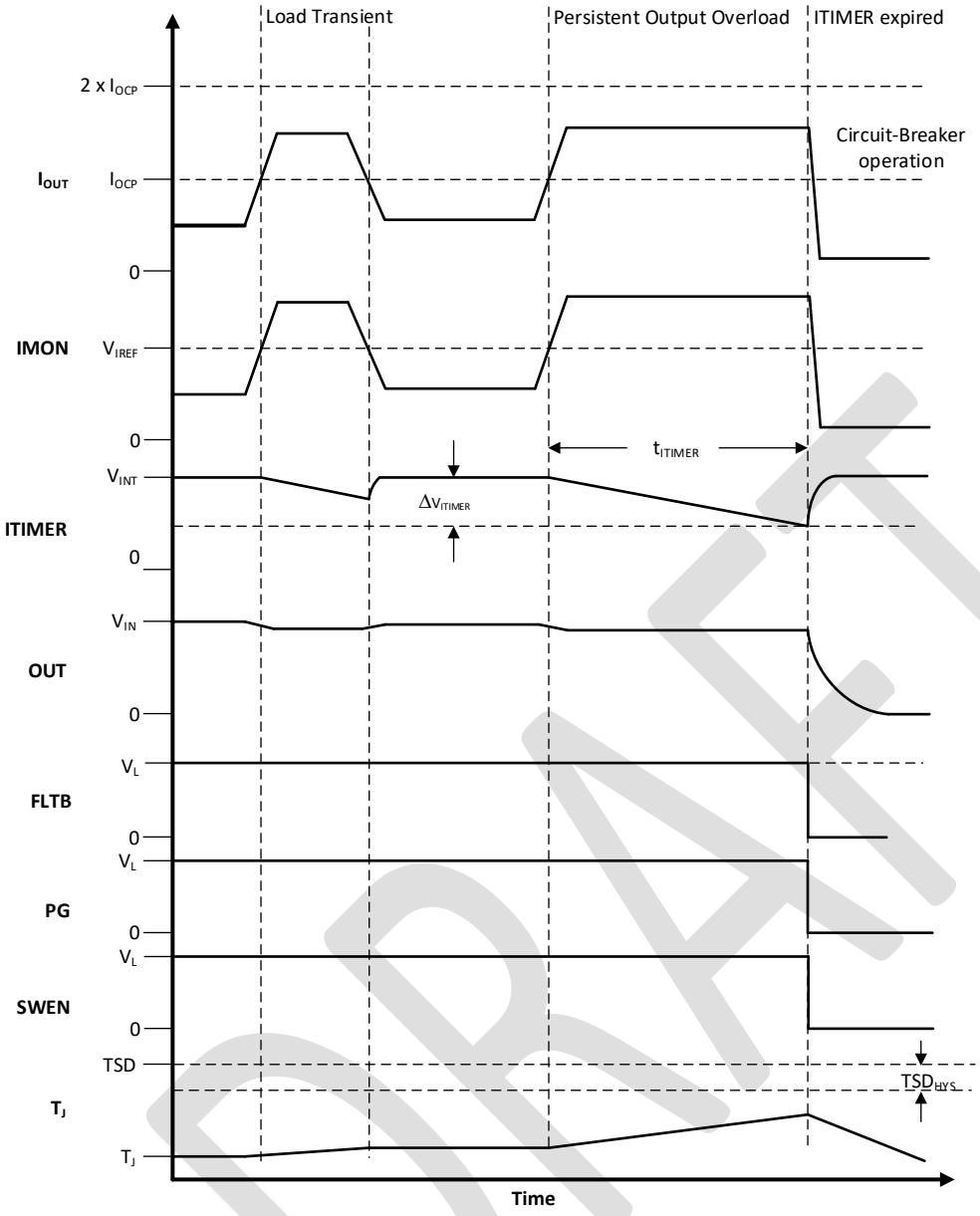


Figure 16 – TPS25984x Overcurrent Response

7.3.3.2.1 IMON pin single point failure

The device relies on the proper R_{IMON} component choice and connection to IMON pin to provide overcurrent protection in steady state. As an added safety measure, it uses the following mechanisms to ensure the device provides some form of overcurrent protection even if the IMON pin is not connected correctly in the system.

IMON pin open: In this case, the IMON pin voltage is internally pulled up to a higher voltage (V_{INT}?) and will exceed the IREF voltage, causing the part to perform a circuit-breaker action even if there's no significant current flowing through the device.

IMON pin shorted to GND: In this case, the IMON pin voltage is pulled to 0 V and will never exceed the IREF voltage, even if there's significant current flowing through the device, thereby rendering the primary circuit-breaker mechanism ineffective. The device relies on a backup overcurrent sense mechanism (OC_BKP) to provide some protection as a back-up. The backup overcurrent threshold is set at 75 A (1.5x max DC current of 50 A). If the device detects that the backup

current sense threshold is exceeded but at the same the OC_IMON is not detected, it triggers pin failure and latches a fault. The FET is turned off and the FLTb pin is asserted.

7.3.3.2.2 ITIMER pin single point failure

The device relies on the proper C_{ITIMER} component choice and connection to ITIMER pin to provide the blanking timer for overcurrent protection in steady state. As an added safety measure, it uses the following mechanisms to ensure the device provides some form of overcurrent protection even if the ITIMER pin is not connected correctly in the system.

ITIMER pin forced to some voltage higher than $V_{ITIMERTHR}$: In this case, the ITIMER pin is unable to discharge and fails to indicate timer expiry, thereby rendering the primary circuit-breaker mechanism ineffective. The device relies on a backup overcurrent timer mechanism (SPFAIL_TMR) to provide some protection as a back-up. The backup timer duration is set at 50 ms (which is higher than the maximum support user adjustable ITIMER). If the device detects an overcurrent event on either the IMON pin (OC_IMON) or the backup OC circuit (OC_BKP), the device engages the SPFAIL_TMR and once the ITIMER expires, it latches a fault - Single point failure (SPFLT). The FET is turned off and the FLTb pin is asserted.

7.3.3.3 Active Current Limiting (I_{LIM})

The TPS25984x responds to output overcurrent conditions during startup by actively limiting the current. The device constantly senses the output load current and provides an analog current output on the ILIM pin which is proportional to the load current, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}).

$$V_{ILIM} = I_{OUT} \times G_{ILIM} \times R_{ILIM}$$

The overcurrent condition is detected by comparing this voltage against a threshold which is a scaled voltage derived from the reference voltage on the IREF pin. The reference voltage (V_{IREF}) can be generated in 2 ways, which changes the overcurrent detection threshold (I_{LIM} or I_{OCP}) accordingly:

1. In standalone mode of operation, the internal current source interacts with the external IREF pin resistor to generate the reference voltage.
$$V_{IREF} = I_{IREF} \times R_{IREF}$$
2. In a primary+secondary configuration, the primary eFuse/controller drives the voltage on IREF pin to provide an external reference (V_{IREF}).

The active current limit threshold during start-up can be calculated as:

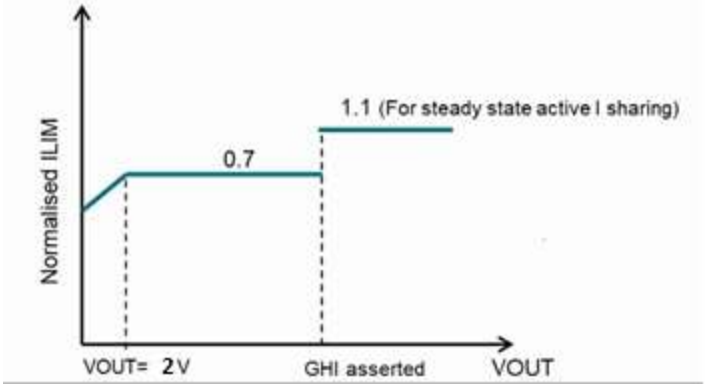
$$I_{LIM} = \frac{0.7 \times V_{IREF}}{3 \times G_{ILIM} \times R_{ILIM}}$$

When the load current exceeds the programmed current limit threshold (I_{LIM}), the device tries to regulate the load current to the programmed current limit (I_{LIM}).

During current regulation, the output voltage will drop resulting in increased device power dissipation across the FET. If the device internal temperature (T_j) exceeds the thermal shutdown threshold (TSD), the FET is turned off. Once the part shuts down due to TSD fault, it would either stay latched off (TPS259840 variants) or restart automatically after a fixed delay (TPS259841 variants). See *Overtemperature Protection* section for more details on device response to overtemperature.

Figure 17 – TPS25984x Overcurrent Response During Start-Up

The active current limit block employs a foldback mechanism during start-up based on the output voltage (VOUT). When VOUT is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.



7.3.3.3.1 ILIM pin single point failure

The device relies on the proper R_{ILIM} component choice and connection to ILIM pin to provide overcurrent protection during inrush. As an added safety measure, it uses the following mechanisms to ensure the device provides some form of overcurrent protection even if the ILIM pin is not connected correctly in the system.

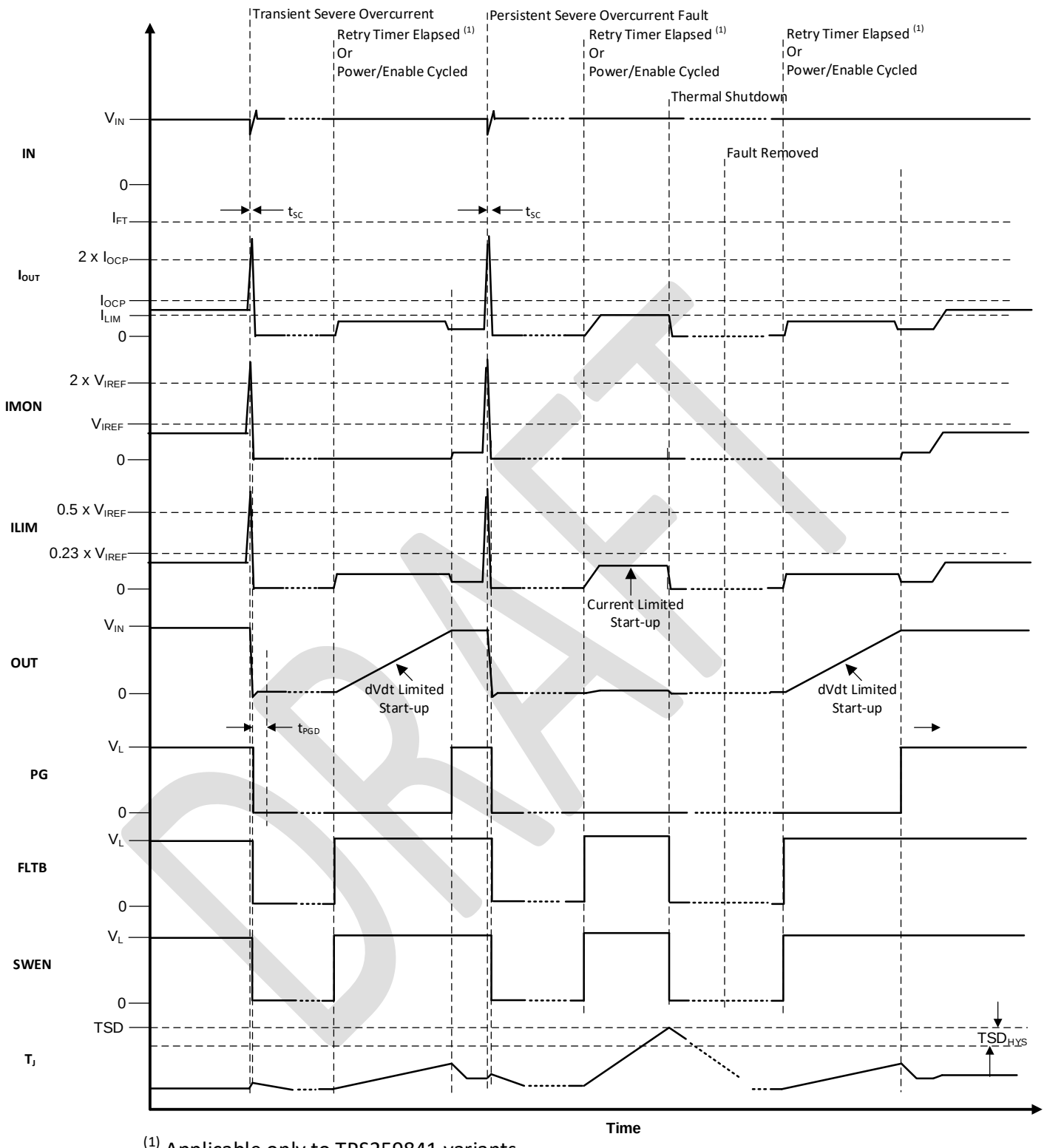
ILIM pin open: In this case, the ILIM pin voltage is internally pulled up to a higher voltage (V_{INT}?) and will exceed the IREF voltage, causing the part to engage current limit even if there's no significant current flowing through the device.

ILIM pin shorted to GND: In this case, the ILIM pin voltage is pulled to 0 V and will never exceed the IREF voltage, even if there's significant current flowing through the device, thereby rendering the primary current limit mechanism ineffective during start-up. The device relies on a secondary current sense mechanism to provide some protection as a back-up. The backup overcurrent threshold (I_{OC_BKP}) is set at 65 A (>> max DC inrush current supported). If the device detects that the backup overcurrent threshold is exceeded but at the same the OC_ILIM is not asserted, it triggers pin failure detection and latches a fault. The FET is turned off and the FLTb pin is asserted.

7.3.3.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast trip comparator triggers a fast protection sequence to prevent the current from building up. The comparator employs a scalable threshold (I_{SFT}) which is equal to 2 × I_{OCP} during steady state and 1.5 x I_{LIM} during inrush. This enables the user to adjust the fast trip threshold as per system rating, rather than using a high fixed threshold which may not be suitable for all systems. Once the current exceeds the fast-trip threshold, the TPS25984x turns off the FET within $t_{FT.}$ The device also employs a higher fixed fast trip threshold (I_{FFT}) to protect fast protection against hard short-circuits during steady state (FET in linear region). Once the current exceeds I_{FFT}, the FET is turned off completely within $t_{FT.}$

In some of the systems, for example blade servers and telecom equipment which house multiple hot-pluggable blades/line cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which could be potentially large enough to trigger the fast trip comparator of the eFuse. The TPS25984x uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating un-interrupted system operation.



(1) Applicable only to TPS259841 variants

Figure 19 – TPS25984x Short Circuit Response

7.3.4 Analog Load Current Monitor (IMON)

The device allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. It also allows the IMON pins of multiple eFuses to be tied together to get the total current in a parallel configuration using TPS25984 with other TPS25984/TPS25990 devices. The IMON signal can be converted to voltage by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}}$$

The TPS25984x IMON circuit is designed to provide high bandwidth and high accuracy across load/temperature, irrespective of board layout and system operating conditions. This allows the IMON signal to be used for advanced dynamic platform power management techniques such as Intel PROCHOT or PSYS to maximize system power utilization and throughput without sacrificing safety/reliability.

NOTE: IMON provides load current monitoring information only during steady state. During inrush IMON reports zero load current.

7.3.5 Unlimited scalability using parallel devices

For systems needing higher current than supported by a single eFuse, multiple eFuses can be connected in parallel to deliver the total system current. Conventional eFuses may not share current equally between themselves during steady state due to mismatches in their path resistances (which includes the individual device Rdson variation from part-to-part, as well as the parasitic PCB trace resistance). This can lead to multiple problems in the system:

1. Some devices will always carry higher current as compared to other devices, which could result in accelerated failures in those devices and overall reduction in system operational lifetime.
2. Thermal hotspots formed on the board on devices and traces/vias carrying higher current, leading to reliability concerns for the PCB. This also makes thermal modeling and board thermal management more difficult for the designer.
3. The devices carrying higher current may hit their individual circuit-breaker threshold even while the total system load current is lower than the overall circuit-breaker threshold. This may lead to false tripping of the eFuse during normal operation. This has an effect of lowering the current carrying capability of the parallel chain. In other words, the parallel eFuse chain current rating needs to be de-rated as compared to the sum of the individual eFuses. This de-rating factor is a function of the path resistance mismatch, number of devices in parallel and the individual eFuse circuit-breaker accuracy.

   The need for de-rating has an adverse impact on the system design. The designer is forced to make one of these trade-offs:
   1. Limit the operating load current of the system to be below the de-rated current threshold. This would mean lower platform capability/throughput than allowed by the power supply (PSU) available.
   2. Increase the overall circuit-breaker threshold to allow the desired system load current to pass through without tripping. As a consequence, the power supply (PSU) needs to be oversized to deliver higher currents during faults to account for the de-grading of the overall circuit-breaker accuracy.

   In either case, the system suffers from poor power supply utilization which could mean sub-optimal system throughput or increased installation/operating costs or both.

The TPS25984x uses a proprietary technique to addresses these problems and provide unlimited scalability of the solution by paralleling as many eFuse as needed, without any degradation in accuracy or unequal current sharing.

For this scheme to work correctly, the devices need to connected in the following manner.

The IMON pins of all the devices need to be connected together. The resistor value on the combined IMON pin can be calculated as:

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOT)}}$$

The R_{ILIM} for each individual eFuse should be selected based on the following equation.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3}$$

Where N = number of devices in parallel chain.

The active current sharing scheme is disengaged when the total system current exceeds the overall circuit-breaker threshold ($I_{OCP(TOT)}$).

7.3.6 FET Health Monitoring

The TPS25984x can detect and report certain conditions which are indicative of failure of the powerpath/FET. These conditions, if undetected/unreported could compromise the system operation either by not delivering power to the load correctly, or not providing the expected level of protection. Once the failure is detected, the TPS25984x turns off the internal FET by pulling the gate low and latches a fault.

D-S short: This could result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at startup by checking if $V_{DS} < V_{DSOK}$ before the FET is turned ON. If yes, the device starts the VDSFLT_TMR and also engages the QOD to try and discharge the output. If the V_{OUT} doesn't fall below V_{FB} before the timer expiry, the device latches a fault (VDSFLT) and asserts the FLTb pin.

G-D short: The TPS25984x detects this kind of FET failure at all times by checking if the gate voltage is close to VIN even when the system is trying to hold the FET in OFF condition (SWEN_SNS = 0).

G-S short: The TPS25984x detects this kind of FET failure during startup by checking if the gate voltage fails to reach the necessary overdrive voltage (GHI) within a certain timeout period (START-UP_TMR) after the gate driver is turned ON (SWEN_SNS = 1). While in steady state (INRUSH_DONE = 1), if GHI goes to 0 when SWEN_SNS = 1, it is latched as a fault without waiting for the timeout period.

7.3.7 Analog Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (Tj) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the controller area of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

Note: The TEMP pin voltage is used only for external monitoring and doesn't interfere with the Overtemperature protection scheme of each individual device which is based purely on the internal temperature monitor.

7.3.8 Overtemperature Protection

Thermal Shutdown will occur when the internal FET becomes too hot to operate safely. When the TPS259840 detects thermal overload (based on absolute temperature or relative thermal gradient), it will be shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS259841 detects thermal overload, it will remain off until it has cooled down sufficiently. Thereafter, it will remain off for an additional delay of t_{RST} after which it will automatically retry to turn on if it is still enabled.

Device	Enter TSD	Exit TSD
TPS259840 (Latch-Off)	$T_J \geq$ TSD or $(T_J - T_A) \geq T_{REL}$ threshold	$T_J <$ TSD - TSD_{HYS} or $(T_J - T_A) < T_{REL}$ and V_{DD} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO Toggled below $V_{SD(F)}$
TPS259841 (Auto-Retry)	$T_J \geq$ TSD or $(T_J - T_A) \geq T_{REL}$ threshold	$T_J <$ TSD - TSD_{HYS} or $(T_J - T_A) < T_{REL}$ and t_{RST} Timer Expired OR V_{DD} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO Toggled below $V_{SD(F)}$

Table – Thermal Shutdown

7.3.9 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions.

Event / condition	Device Response	Fault latched internally	$\overline{FLT}$ Pin	$\overline{FLT}$ Delay
Steady State	None	N	H	
Inrush	None	N	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	H	
Transient Overcurrent	None	N	H	
Persistent Overcurrent (Steady state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent Overcurrent (Inrush)	Current Limit	N	L	
Short-Circuit (primary mode)	Fast-trip	Y	L	t_{FT}
Short-Circuit (secondary mode)	Fast-trip followed by Current Limited Startup	N	H	
ILIM Pin Open (Inrush)	Shutdown	Y	L	
ILIM Pin Short (Inrush)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	
ILIM Pin Open (Steady state)	Active current sharing loop always active	N	H	
ILIM Pin Short (Steady state)	Active current sharing loop disabled	N	H	
IMON Pin Open (Steady state)	Shutdown	Y	L	
IMON Pin Short (Steady state)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	
IREF Pin Open (Inrush)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	
IREF Pin Open (Steady state)	Shutdown (If $I_{OUT} > I_{OC\_BKP}$)	Y	L	t_{ITIMER}
IREF Pin Short (Steady state)	Shutdown	Y	L	
IREF Pin Short (Inrush)	Shutdown	Y	L	
ITIMER pin forced to high voltage	Shutdown (If $I_{OUT} > I_{OCP}$ or $I_{OUT} > I_{OC\_BKP}$)	Y	L	t_{SPFAIL_TMR}
Start-up Timeout	Shutdown	Y	L	t_{SU_TMR}
FET Health Fault (G-S)	Shutdown	Y	L	10 us??
FET Health Fault (G-D)	Shutdown	Y	L	
FET Health Fault (D-S)	Shutdown	N	L	t_{SU_TMR}
External Fault (SWEN pulled low externally while device is not in UV/OV)	Shutdown	Y	L	

Table – Fault Summary

NOTE: The $\overline{FLT}$ is an open-drain pin and needs to be pulled up to an external supply.

The device response after a fault varies based on the mode of operation:

1. During standalone/primary mode of operation (MODE = OPEN), the device latches a Fault and follows the Auto-retry/Latch-off response as per the device selection. When the devices turns on again, it follows the usual DVDT limited start-up sequence.

2. During secondary mode of operation (MODE = GND), after the fast-trip, the device pulls the SWEN pin low initially to signal the event to the primary device. It then waits for a short de-glitch interval (10us) for the primary device to register the event and take control of the SWEN thereafter. It then releases the SWEN pin internal pull-down and samples the SWEN pin externally to verify that the primary device has indeed taken control and pulled it low. If the primary device is unable to control the SWEN pin, it goes high. The secondary device detects this event as a fault and remains latched-off. Thereafter, the device can be turned on again only by power cycling VDD below V_{UVP} or by cycling EN/UVLO pin below V_{SD}.

For faults which are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below V_{SD} clears the fault and the $\overline{FLT}$ pin is de-asserted. It also clears the t_{RST} timer (Auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both Latch-off & Auto-retry variants.

When there is no supply to the device, the $\overline{FLT}$ pin is expected to stay low to indicate a UVLO fault. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the $\overline{FLT}$ pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.3.10 Parallel Device Synchronization (SWEN)

The SWEN pin is a signal which is driven high when the FET needs to be driven to ON state. When it is driven low (internally or externally), it forces the driver circuit to keep the FET in OFF condition. This allows multiple devices in a parallel configuration to synchronize the ON/OFF transitions.

Device state	FET driver status	SWEN
Steady State	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Insertion delay	OFF	L
Overvoltage Lockout (VIN OVP)	OFF	L
Transient Overcurrent	ON	H
Circuit-Breaker (Persistent Overcurrent followed by ITIMER Expiry)	OFF	L
Fast-trip	OFF	L
Fault response Mono-shot running (MODE = GND)	OFF	L
Fault response Mono-shot expired (MODE = GND)	ON	H

ILM Pin Open (Inrush)	OFF	L
ILM Pin Short (Inrush)	OFF	L
ILM Pin Open (Steady state)	OFF	L
ILM Pin Short (Steady state)	OFF	L
FET Health Fault	OFF	L

Table – SWEN Summary

The SWEN is an open-drain pin and needs to be pulled up to an external supply.

The SWEN pin has an internal timeout circuit. If the SWEN is held low (internally or externally) for an extended period of time (t_{SWENTO}), it resets the logic (FAST_REC = 0) so that the next time the device starts up after SWEN goes high, it follows the normal inrush sequence. In other cases, it may bypass the inrush sequence and perform a current limited startup for fast recovery.

During a fault, secondary device pulls the SWEN low and also latches a fault internally. It then waits for a short time (10 us) for the primary to latch the fault and releases the SWEN pull-down. It then samples the SWEN pin status to check if primary has registered the fault and is holding it low. If yes, it resets the internal fault and thereafter relies on SWEN from primary to determine if it needs to remain off or turn on again. However, if the primary device fails to register the fault and keep the SWEN low, the secondary device enters a latched-off condition till a power/enable cycle event.

It's recommended to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.

7.3.11 Power Good Indication (PG)

This is an active high output which is asserted high to indicate when the device is in steady state and capable of delivering maximum power.

Event	FET Status	PG Pin	PG Delay
Undervoltage (V_{DD}/V_{IN} < V_{UVP} or V_{EN} < V_{UVLO})	OFF	L	t_{PGD}
Overvoltage (V_{IN} > V_{OVP})	OFF	L	t_{PGD}
Steady State	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient Overcurrent	ON	H	N/A
Circuit-Breaker (Persistent Overcurrent followed by ITIMER Expiry)	OFF	L (MODE = H) H(MODE = L)	t_{PGD} N/A
Fast-trip	OFF	L (MODE = H) H(MODE = L)	t_{PGD} N/A
ILM Pin Open	OFF	L (MODE = H) H(MODE = L)	t_{ITIMER} + t_{PGD} N/A
ILM Pin Short	OFF	L (MODE = H) H(MODE = L)	t_{PGD} N/A
Overtemperature	Shutdown	L (MODE = H) H(MODE = L)	t_{PGD} N/A

Table – TPS25984x PG Indication Summary

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. The PG assertion is based on internal GHI. When the FET gate voltage reaches the

full overdrive ($V_{GS} > V_{GS(GHI)}$) indicating that the inrush sequence is complete and device is capable of delivering full power PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation if the FET is turned OFF. The PG de-assertion de-glitch time is t_{PGD}.

The PG is an open-drain pin and needs to be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

When the device is used in secondary mode (MODE = GND) in conjunction with another TPS25984/TPS25990 device as the primary device in a parallel chain, it controls the PG assertion during start-up, but once the device reaches steady state, it no longer has control over the PG de-assertion. Please refer to the ***MODE configuration*** section for more details.

7.3.12 Output Discharge (QOD)

The device has integrated output discharge function. The internal OQD pull-down FET on the OUT pin is activated when the EN/UVLO is held low ($V_{SD} < V_{EN} < V_{UVLO}$) for a minimum interval (t_{QOD}), or if the VDS is lower than (V_{DSOK}) when SWEN is made high after being held low for a minimum interval (t_{SWENTO}). The output discharge function is helpful in quickly removing residual charge left on the large output capacitors and avoids bus floating at some undefined voltage. The output discharge function may result in excess power dissipation inside the device leading to increase in junction temperature (Tj). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long term degradation of the part. The QOD pull-down is disengaged when $V_{OUT} < V_{FB}$ or if the device detects a Fault.

7.3.13 Mode configuration (MODE)

This pin can be used to configure the TPS25984 as a secondary device in a chain along with a primary device such as TPS25990 or another TPS25984. This allows some of the TPS25984 pin functions to be changed to aid the primary-secondary configuration.

This pin is sampled once at power up. Leaving it open configures it as a primary/standalone device. Connecting this pin to GND configures it as a secondary device.

Following functions are disabled in secondary mode and the device relies on the primary device to provide this functionality:

1. IREF internal current source
2. DVDT internal current source
3. Circuit-breaker
4. PG de-assertion (pull-down) after reaching steady state
5. Latch-off after fault

In secondary mode, following functions are still active:

1. Thermal protection
2. Start-up current limit based on ILIM
3. Active Current Sharing during inrush as well as steady state
4. Current Monitor (IMON) in steady state
5. Steady state overcurrent detection based on IMON. Indicated by pulling ITIMER pin low, but doesn't trigger CB action on ITIMER expiry. Rather, it relies on the primary device to start its own ITIMER and then trigger the CB action for the whole chain by pulling SWEN low after the ITIMER expiry. However, the secondary devices use an internal overcurrent timer (SPFAIL_TMR) as backup in case the primary fails to initiate CB action for an extended period of time.
6. Each device will still have individual Scalable and Fixed fast trip to protect itself. The individual SCP is set to max i.e. 2 x I_{OCP} (steady state) or 2 x I_{LIM} (Inrush) in secondary mode so that the primary device can lower it further for the whole system if configured through PMBus.

7. Individual OVP is set to maximum in secondary device so that the primary can lower it further for the whole system if configured through PMBus.
8. FLTb assertion based on individual device fault detection (except CB)
9. PG de-assertion control during inrush and assertion control after device reaches steady state. However, once in steady state, the secondary device no longer controls the de-assertion of the PG in case of faults.
10. SWEN assertion/de-assertion based on internal events as well as FET ON/OFF control based on SWEN pin status

In secondary mode, the device behavior during short-circuit fast-trip is also altered. More details available in the short-circuit protection section.

7.4 Device Functional Modes

The features of the device depend on the operating mode. Table below summarizes the Device Functional Modes:

Pin: EN/UVLO	Device State	QOD
> V_{UVLO}	Fully ON	Disabled
> V_{SD} , < V_{UVLO}	FET OFF	Enabled
< V_{SD}	Shutdown	Disabled

Pin: MODE	Device Configuration
Open	Primary/Standalone
GND	Secondary

8 Applications and Implementation

The TPS25984x can be used in a variety of configurations.

8.1 Single Device, Self-Controlled

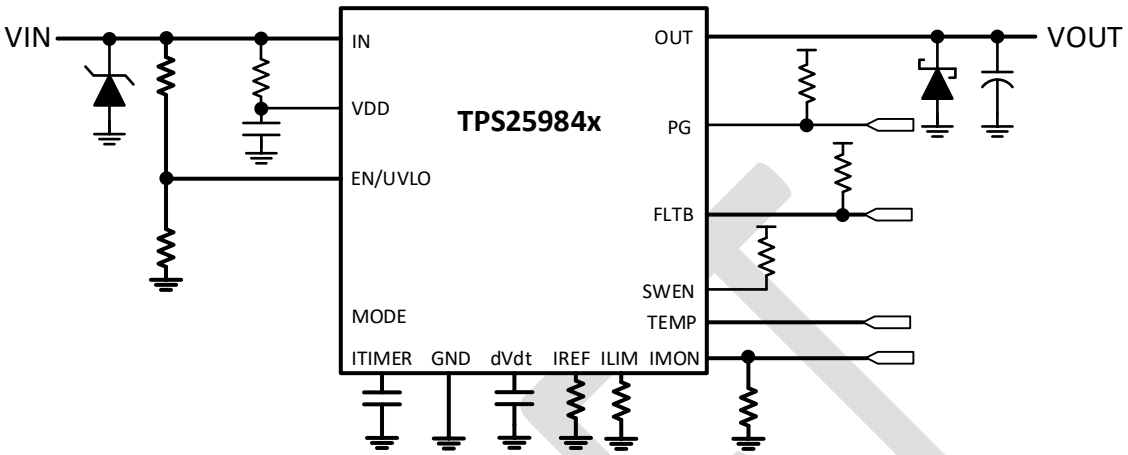


Figure – Single Device, Self-Controlled

The MODE pin is left OPEN to configure for standalone operation.

Other variations:

1. The IREF can be driven from an external reference voltage source.
2. In a Host controlled system, EN/UVLO or OVP can also be driven from the host GPIO to control the device. IMON pin voltage can be monitored using Host ADC. The Host can use a DAC to drive IREF to change the current limit threshold on the fly.
3. The device can be used a simple load switch without adjustable overcurrent/fast-trip protection by tying the ILIM/IMON pin to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.

8.1.1 Multiple devices, Parallel operation

Applications which need higher current capability can use 2 or more TPS25984x devices connected in parallel as shown below.

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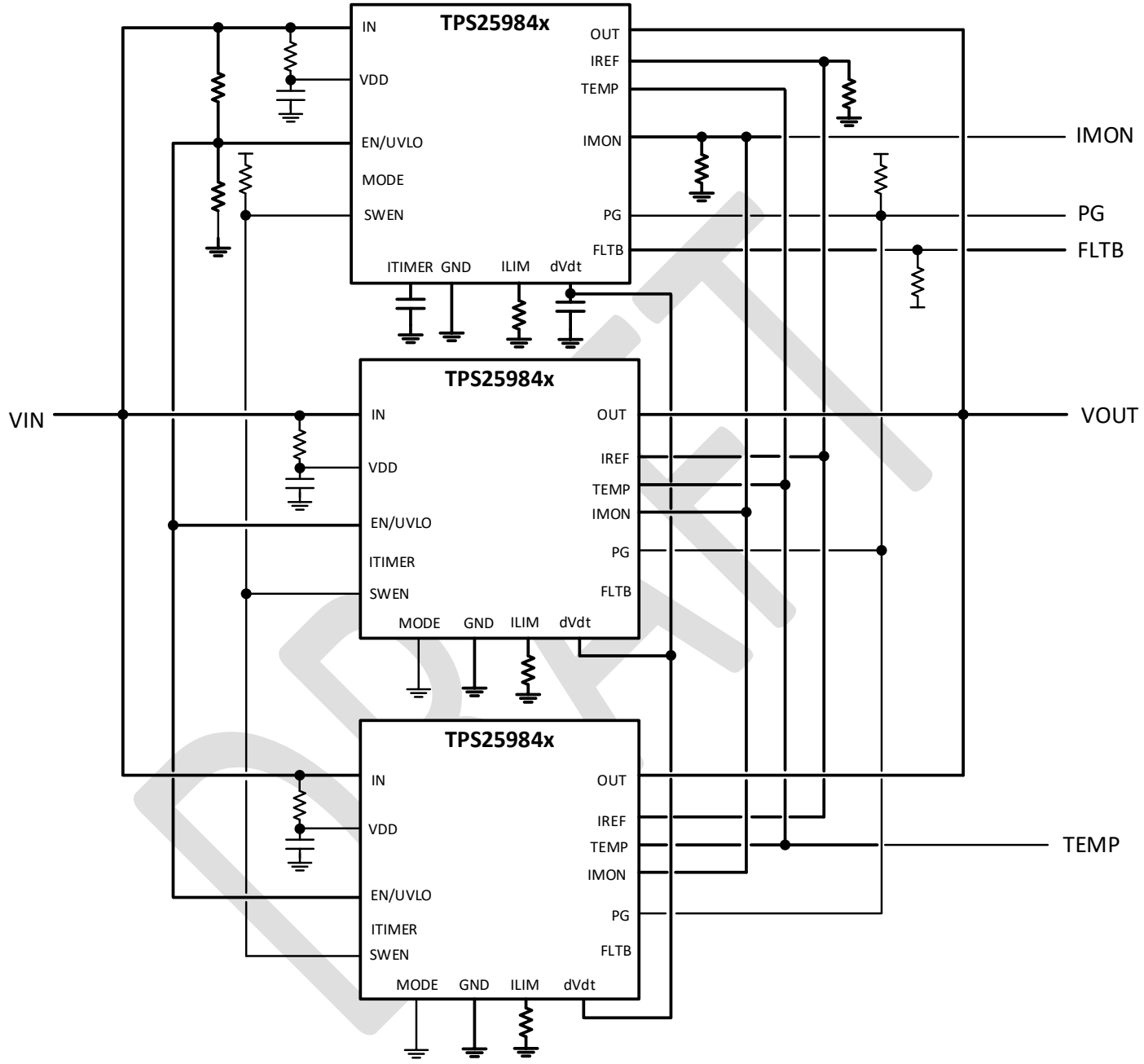


Fig Devices connected in parallel for higher current capability

In this configuration, one TPS25984x device is designated as the primary device and controls the other TPS25984x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through a R-C filter
2. MODE pin is left OPEN

3. ITIMER is connected through capacitor to GND
4. DVDT is connected through capacitor to GND
5. IREF is connected through resistor to GND
6. IMON is connected through resistor to GND
7. ILIM is connected through resistor to GND
8. SWEN is pulled up to a 3.3V/5V rail using a 10K resistor

The secondary devices have the following connections:

1. VDD is connected to IN through a R-C filter
2. MODE pin is connected to GND
3. ITIMER pin is left OPEN
4. ILIM is connected through resistor to GND

The following pins of all devices are tied together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. SWEN
6. PG
7. IMON
8. IREF

In this configuration, all the devices are powered up and enabled simultaneously.

Power up: After power up/enable, initially all devices hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. Once all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs.

Inrush: During inrush, since the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{dVdt}) as per the following equation:

$$SR\,(mV/\mu s) = \frac{I_{INRUSH}(mA)}{C_L\,(\mu F)}$$

$$C_{DVDT}\,(pF) = \frac{42000}{SR\,(mV/\mu s)}$$

In this condition, the internal balancing circuit ensures that the load current is shared equally among all devices during start-up. This prevents a situation where some devices turn on faster than others and see more thermal stress as compared to other devices, which could potentially result in pre-mature or partial shutdown of the parallel chain, or even SOA damage to the devices. Active current sharing ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful startup with larger output capacitances or higher loading during startup.

All devices hold their respective PG signals low during startup. Once the output ramps up fully and reaches steady state, each device releases its own PG. Since the DVDT pins of all devices are tied together, the internal GHI of all devices is synchronized. There could be some threshold/timing mismatches between devices leading to PG assertion in a staggered manner. However, since the PG pins of all devices are tied together, the combined PG signal goes high only once all devices have released their PG, signaling the downstream load that it's okay to draw power.

Steady State: During steady state, all devices share current equally using the active current sharing mechanism which actively regulates the respective device Rdson to evenly distribute current across all the devices in the parallel chain.

Overcurrent during steady state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than individual device. This is done by connecting the IMON pins of all the devices together. Similarly, the IREF pins of all devices are tied together and connected to a single R_{IREF} to generate a common reference for the overcurrent protection block in all the devices. This helps reduce the contribution of I_{IREF} variation and R_{IREF} tolerance to the overall mismatch in overcurrent threshold between devices. In this case, choose the combined R_{IMON} as per the following equation:

$$R_{IMON} = \frac{I_{IREF} \times R_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}}$$

The R_{ILIM} for each individual eFuse should be selected based on the following equation.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3}$$

Where N = number of devices in parallel chain.

Other variations:
The IREF can be driven from an external voltage reference (V_{IREF}).

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}}$$

During an overcurrent event, the overcurrent detection of all the devices are triggered simultaneously. This in turn triggers the overcurrent blanking timer (ITIMER) on each device. However, only the primary devices uses the ITIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain. However, the secondary devices also start their backup overcurrent timer (SPFAIL_TMR) and can trigger the shutdown of the whole chain if the primary device fails to do so in time.

This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and ITIMER intervals between devices don't degrade the accuracy of the circuit-breaker threshold of the parallel chain or the overcurrent blanking interval, which is undesirable.

Severe Overcurrent (Short-circuit): If there's a severe fault at the output (e.g. output shorted to ground with a low impedance path), during steady state operation, the current builds up very quickly to a high value and triggers the fast-trip response in each device. The devices use 2 thresholds for fast-trip protection – an user adjustable threshold (I_{SFT} = 2 x I_{OCP} in steady state or I_{SFT} = 1.5 x I_{LIM} during inrush) as well as a fixed threshold (I_{FFT} = V_{DSCOMP}/R_{ON}, only during steady state). After the fast-trip, the devices enter a latch-off fault condition till the device is power cycled or re-enabled or after expiry of auto-retry timer (only for auto-retry variants).

8.1.2 Multiple devices, Parallel operation with Digital Communication interface

Systems which need higher current along with digital interface for telemetry, control, configurability can use TPS25984 device(s) in parallel with TPS25990 to increase the current capability. TPS25990 is an integrated eFuse with PMBus digital interface which can act as the primary controller in a parallel eFuse configuration.

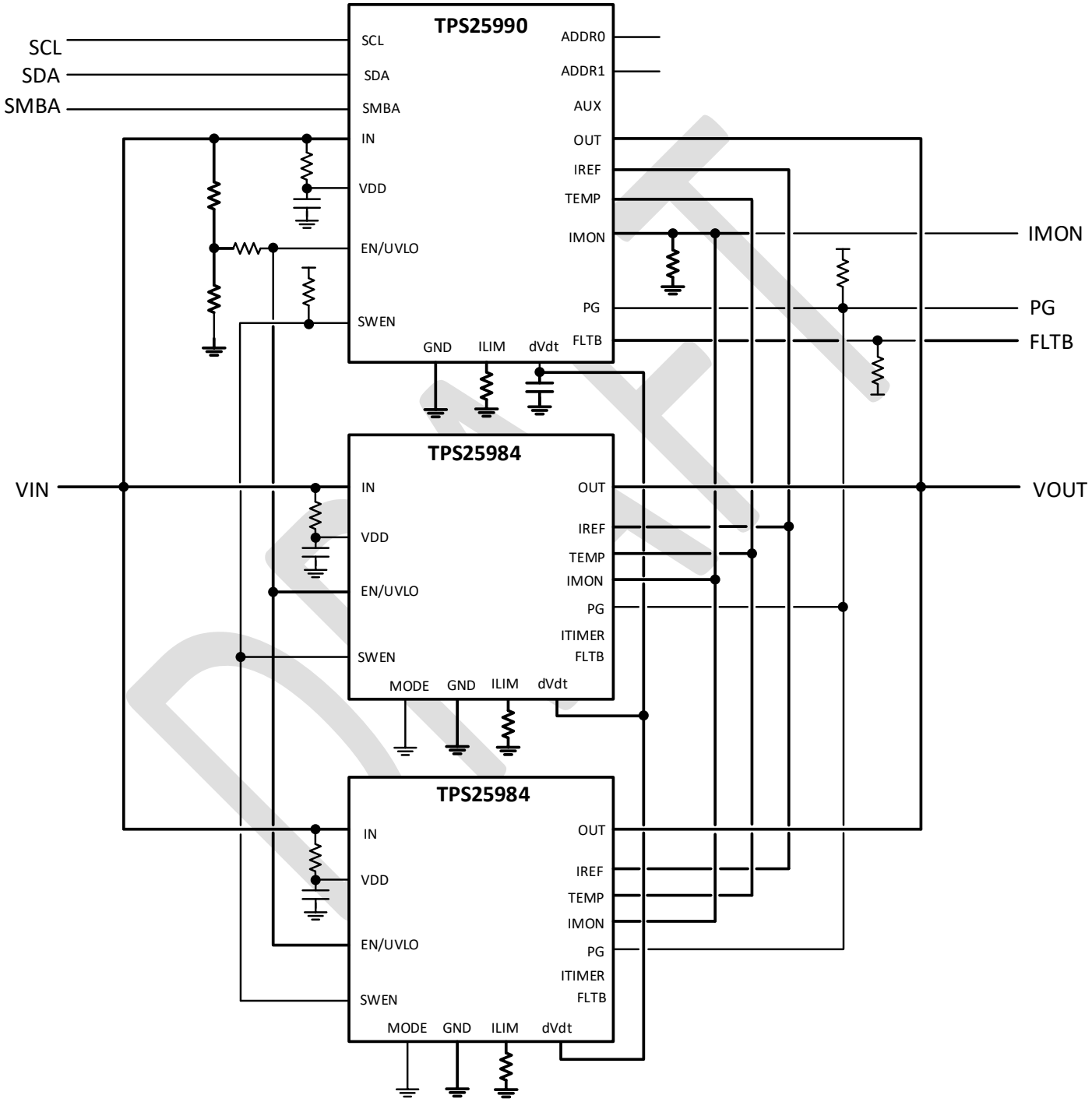


Fig Devices connected in parallel for higher capability along with Telemetry Controller eFuse

This configuration is quite similar to the previous configuration using multiple TPS25984 devices. The connections for individual secondary devices as well as their connection to the primary device are identical, with the following changes:

1. The TPS25990 is used as the primary device in place of TPS25984
2. The TPS25990 monitors the combined VIN, VOUT, IMON, TEMP and reports it over the PMBus telemetry interface.
3. The TPS25990 uses the SWEN pin to control the other devices in the chain according to the PMBus ON/OFF control commands.
4. THE OVP threshold is set to max value in all devices by default. For TPS25984 devices, the OV threshold is fixed in hardware and cannot be changed. The TPS25990 OV threshold can be lowered through PMBus. In this case, the TPS25990 use the SWEN pin to turn off the TPS25984 devices during OV conditions.
5. THE UVLO threshold for all devices is set by the external resistor divider from IN to GND on the EN/UVLO pin. The TPS25990 UV threshold can be increased through PMBus. In this case, the TPS25990 use the SWEN pin to turn off the TPS25984 devices during UV conditions.
6. During inrush, the output of all the devices are ramped together based on the DVDT cap. However, the TPS25990 DVDT sourcing current can be configured through the PMBus to change the inrush behavior of the whole chain.
7. Due to the inherent difference in Rdson, the current carried by the TPS25990 is lower than the TPS25984 devices. Accordingly, the OC threshold for the TPS25990 has to be set to a relatively lower value as compared to all the TPS25984 devices by connecting a proportionately higher ILIM resistor.
8. The TPS25990 controls the overall OC threshold of the parallel chain by setting the IREF threshold voltage using its internal DAC. The IREF voltage can be configured through PMBus to change the OC threshold digitally.
9. Once the TPS25990 detects an overcurrent even during steady state, it starts an internal overcurrent timer which is digitally programmable. Once the digital timer expires, the TPS25990 pulls the SWEN pin low to signal all devices in the chain to break the circuit simultaneously.
10. The TPS25990 generates the Power Good (PG) indication for the whole system. The TPS25990 PG assertion is based on internal GHI ($V_{GS} > V_{GS(GHI)}$) and V_{OUT} PG threshold (PGTH) which is digitally programmable. The TPS25984 secondary devices have control over the system PG assertion only during start-up. Once in steady state, only the TPS25990 controls the de-assertion of the PG based on the PG threshold.

9 Power Supply Recommendations

The TPS25984x devices are designed for a supply voltage range of 4.5 - 16 V on the IN and VDD pins. It's recommended to use a minimum capacitance of 0.1uF on the IN pin to avoid coupling of high slew rates during hotplug events. It's recommended to use a R-C filter from the input supply to the VDD pin to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

10 Layout Recommendations

• For all applications, a ceramic decoupling capacitor of 0. 1 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
• The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
• High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
• The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
• The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias .
• Locate the following support components close to their connection pins:
– R_{ILIM}
– R_{IMON}
– R_{IREF}
– C_{dVdT}
– C_{ITIMER}
– Resistors for the EN/UVLO pin
Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft start timing. These traces must not have any coupling to switching signals on the board.
• It's recommended to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.
• Since the IMON, ILIM and IREF pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
• Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

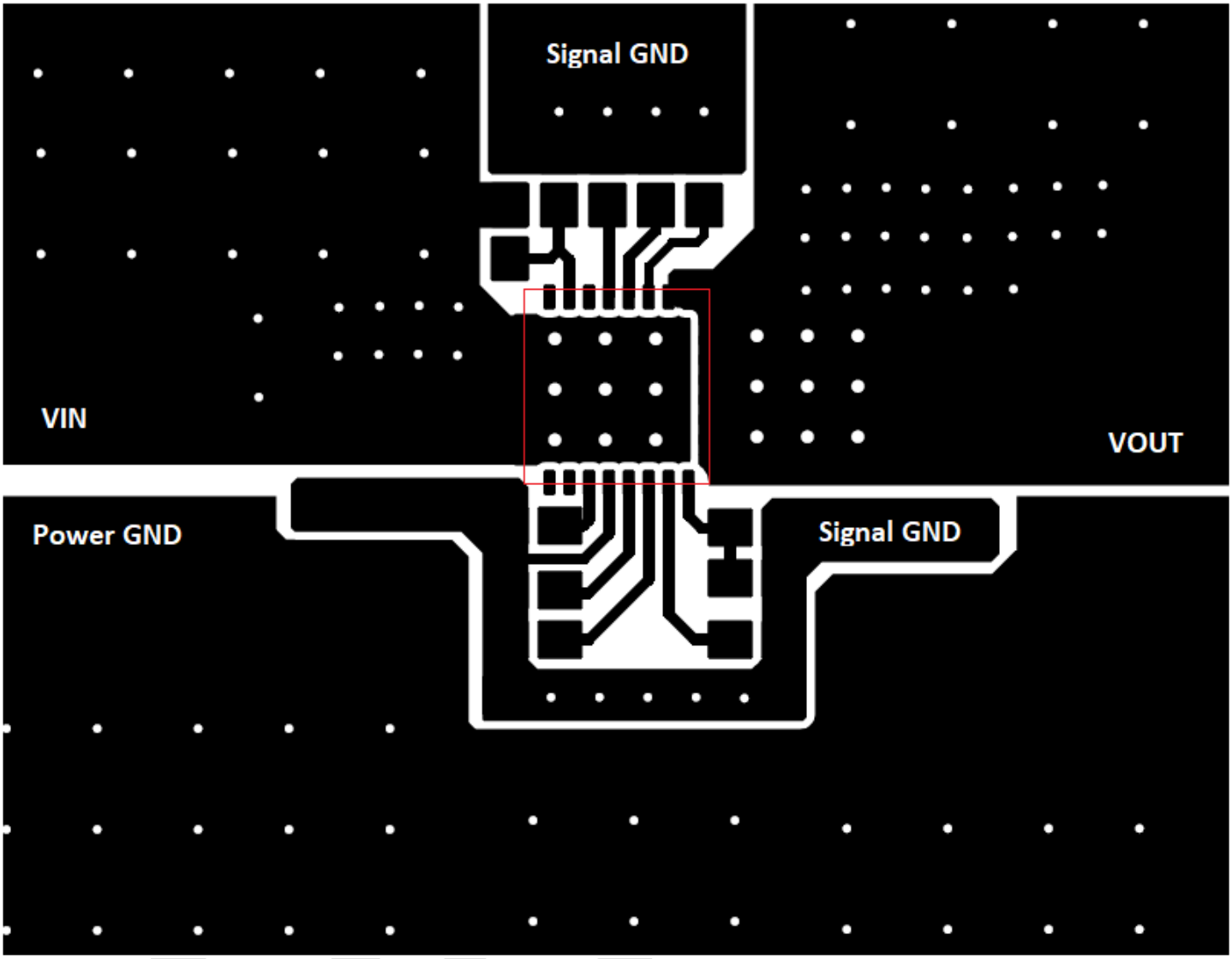
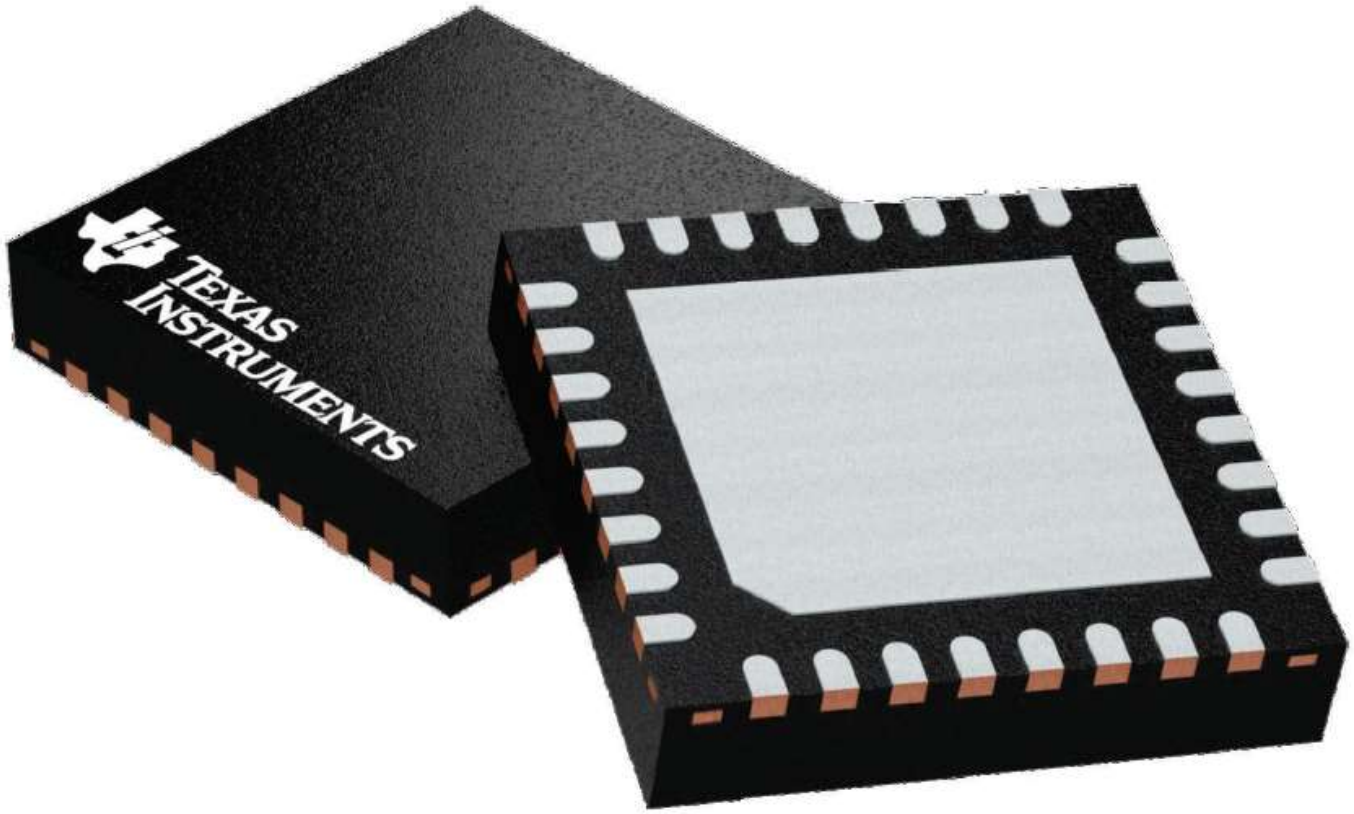


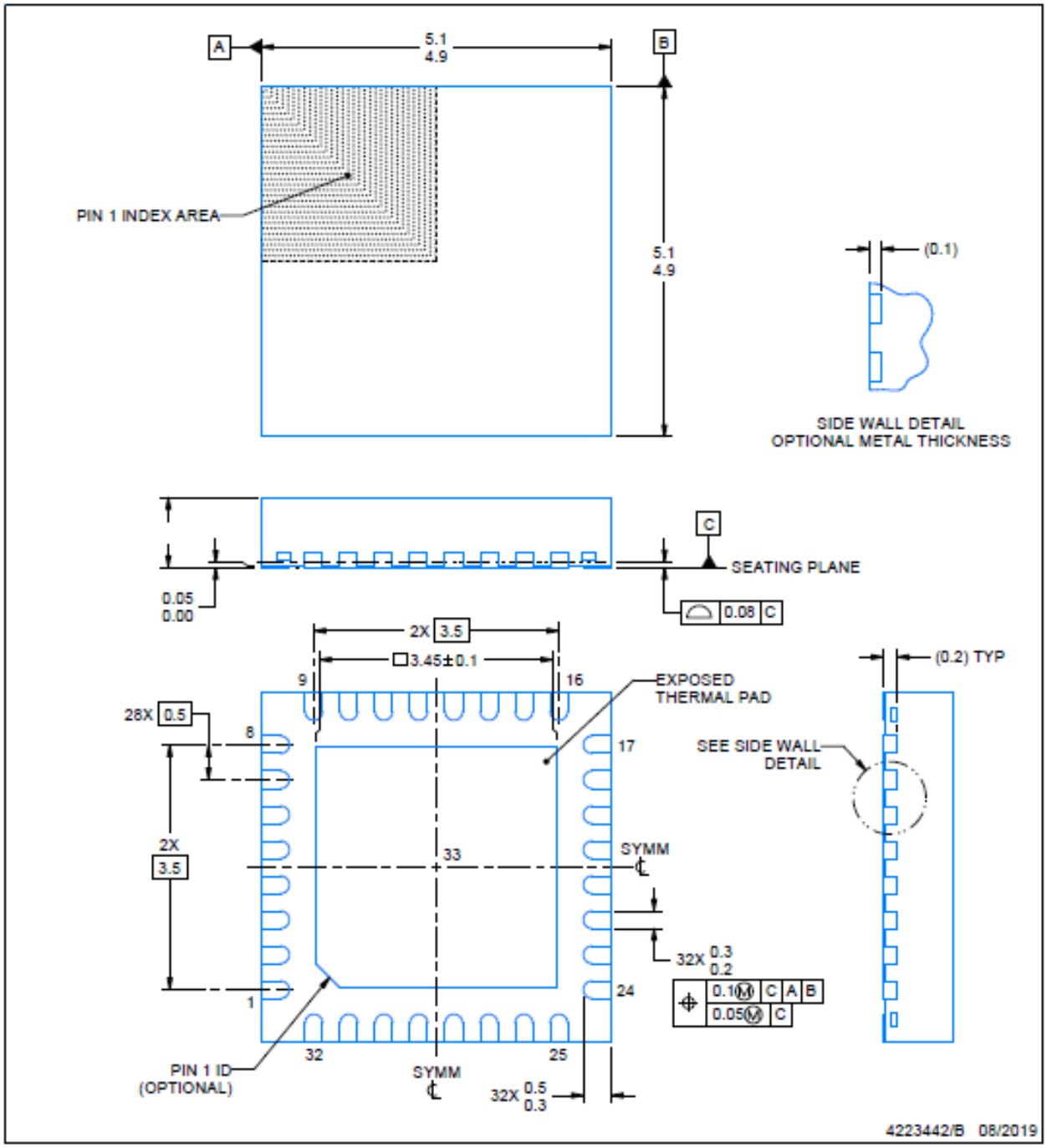
Figure 27 - Layout example

11 Package and Mechanical Drawings



PACKAGE OUTLINE

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.