The following are the settings and adjustments I made on the TPS2640 EVM.

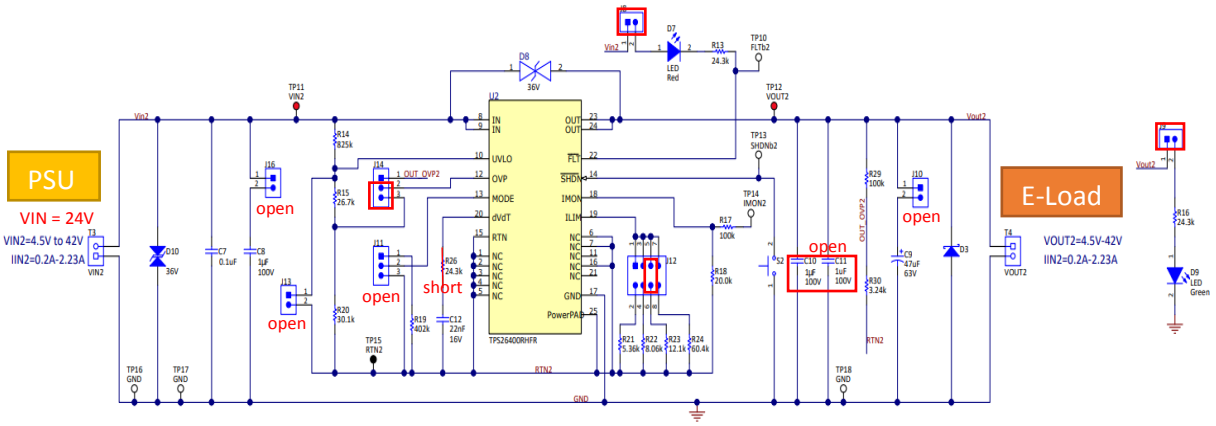
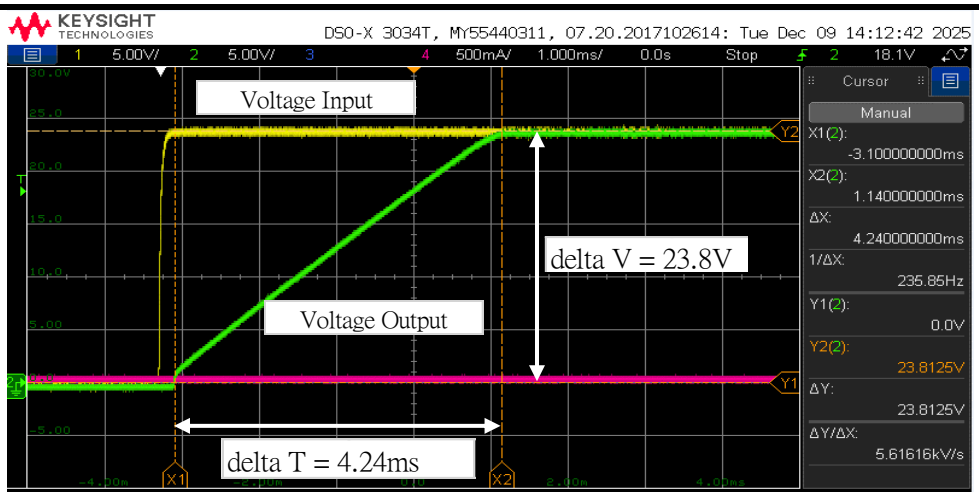


Figure 3-1. TPS2640EVM Schematic

Test Item	Verify the TPS2640 output voltage slew rate during start-up

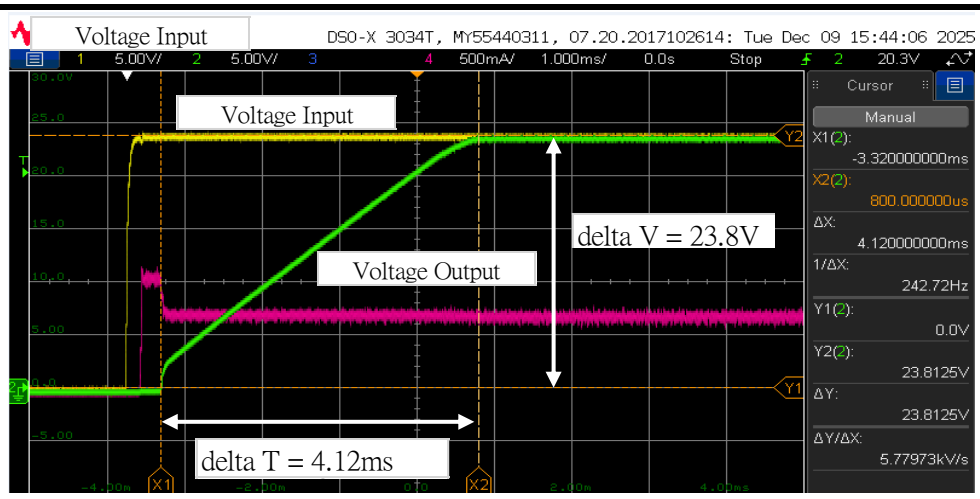
Test method 1:	Input voltage at 24V, no load.



Spec	24V / 4.224ms

Test summary:	Verification is correct and matches the specification.

Test method 2:	Input voltage at 24V, have load.

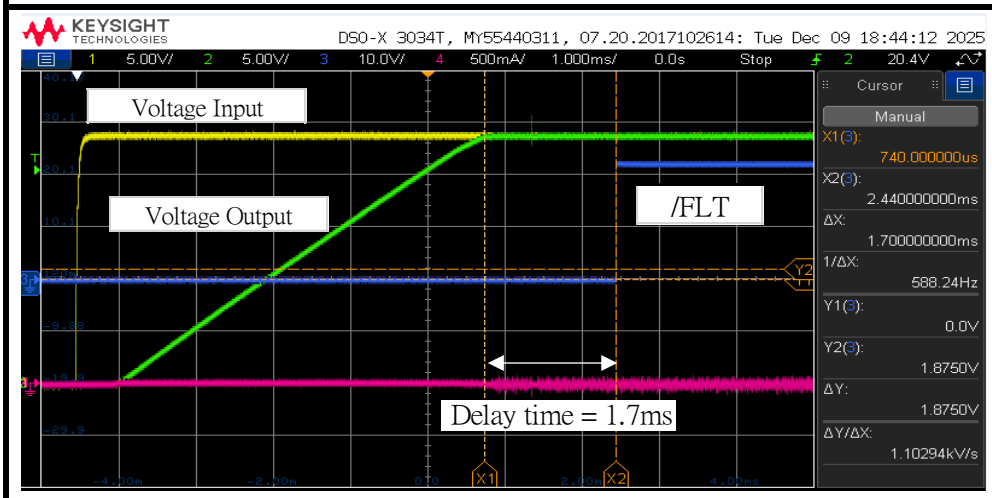


Spec	24V / 4.224ms

Test summary:	Verification is correct and matches the specification.

Test Item	Verify the TPS2640 Power Good indicator signal transitioning from low to high.

Test method 1: Input voltage at 24V, no load.



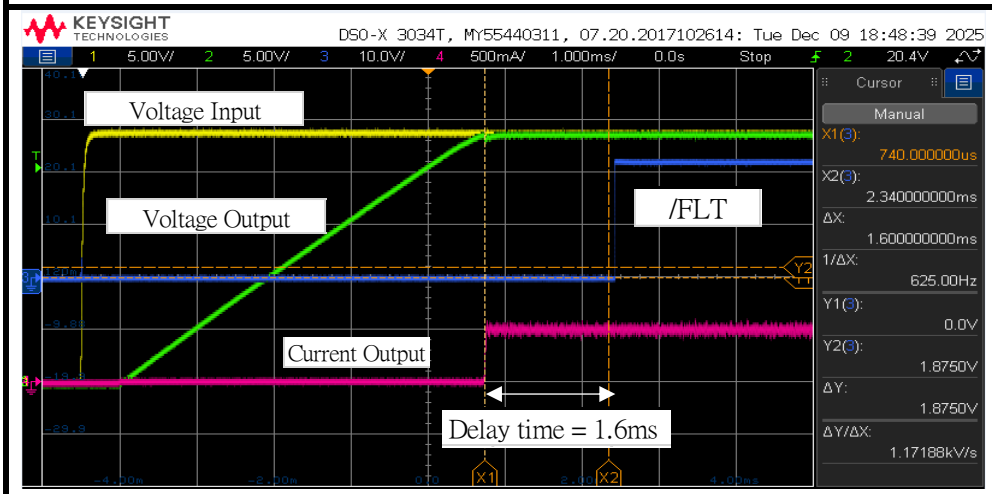
Spec					
t_{PGOODF} / t_{PGOODR}	PGOOD delay (de-glitch) time	Falling edge	875	μs
		Rising edge, $C_{(dV/dT)}$ = open	1400	
		Rising egde, $C_{(dV/dT)}$ ≥ 10 nF, [$C_{(dv/dt)}$ in nF]	875 + 20 × $C_{(dV/dT)}$	

Test summary:

tPGOODR is = 875 + 20 * 22nF = 1315us

The test result is 1.7ms does not meet the specification.

Test method 2: Input voltage at 24V, have load 0.5A.



Spec					
t_{PGOODF} / t_{PGOODR}	PGOOD delay (de-glitch) time	Falling edge	875	μs
		Rising edge, $C_{(dV/dT)}$ = open	1400	
		Rising egde, $C_{(dV/dT)}$ ≥ 10 nF, [$C_{(dv/dt)}$ in nF]	875 + 20 × $C_{(dV/dT)}$	

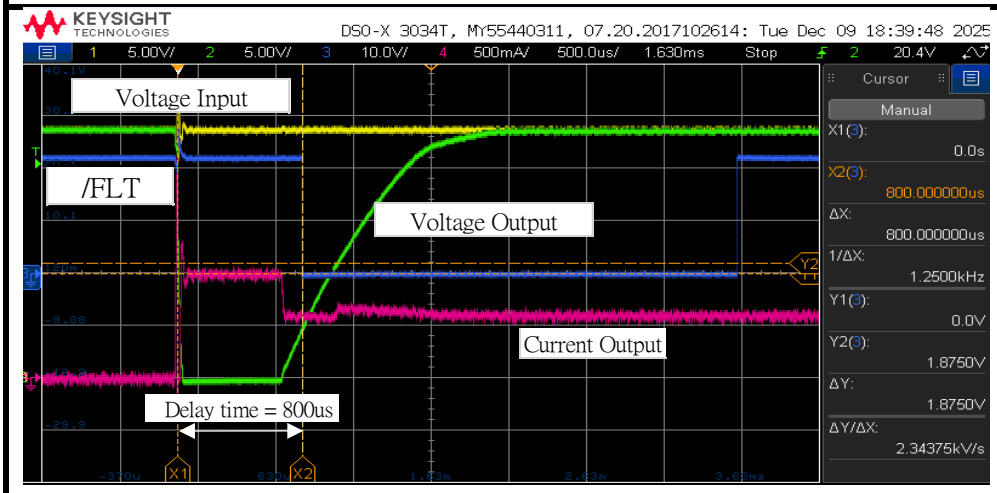
Test summary:

tPGOODR is = 875 + 20 * 22nF = 1315us

The test result is 1.6ms does not meet the specification.

Test Item	Verify the TPS2640 Power Good indicator signal transitioning from high to low.

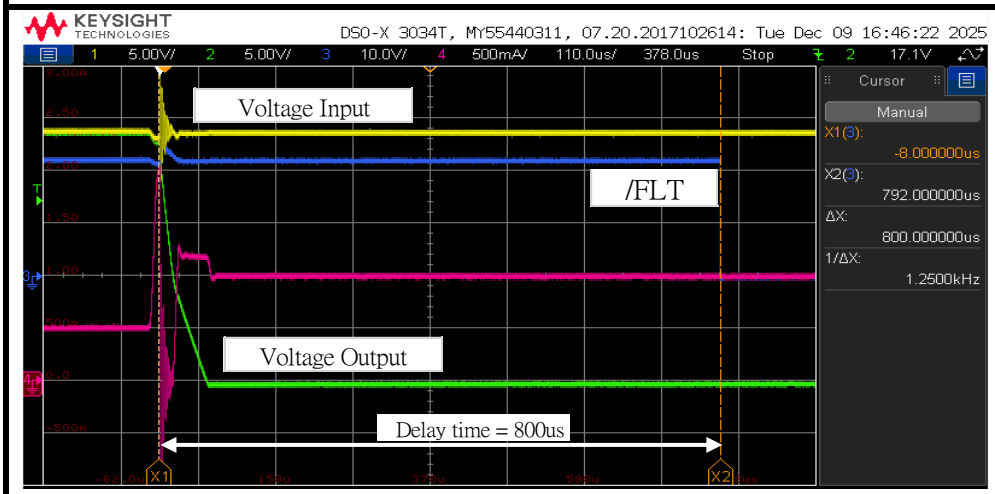
Test method 1:	With an input voltage of 24V and I(FASTRIP) = 1.87A, apply a 2A load using the electronic load, then reduce the load back to 0.5A.



Spec					
	t_{PGOODF}	PGOOD delay (de-glitch) time	Falling edge	875	µs
	t_{PGOODR}		Rising edge, $C_{(dV/dT)}$ = open	1400	
			Rising egde, $C_{(dV/dT)}$ ≥ 10 nF, [$C_{(dv/dt)}$ in nF]	875 + 20 × $C_{(dV/dT)}$	

Test summary:	tPGOODF is = 875us The test result is 800us does not meet the specification.

Test method 2:	With an input voltage of 24 V and I(FASTRIP) = 1.87 A, apply a 0.5A load using the electronic load, then increase the load to 2A.

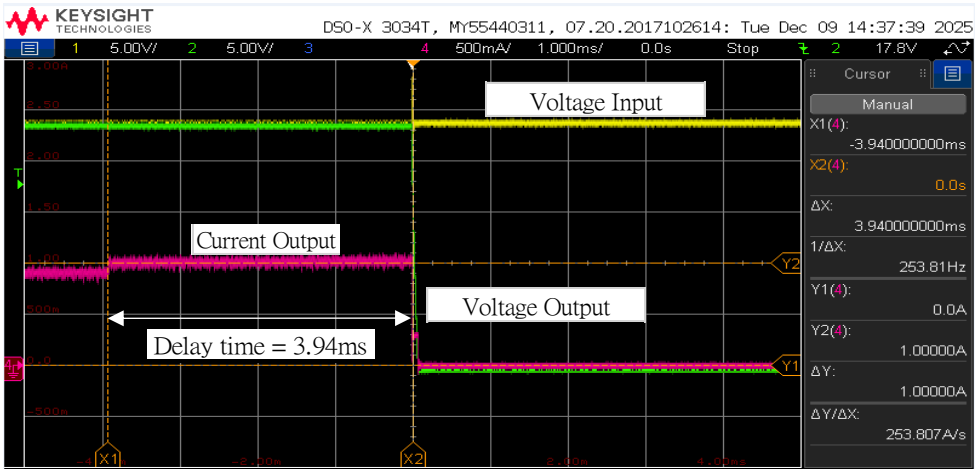


Spec					
	t_{PGOODF}	PGOOD delay (de-glitch) time	Falling edge	875	µs
	t_{PGOODR}		Rising edge, $C_{(dV/dT)}$ = open	1400	
			Rising egde, $C_{(dV/dT)}$ ≥ 10 nF, [$C_{(dv/dt)}$ in nF]	875 + 20 × $C_{(dV/dT)}$	

Test summary:	tPGOODF is = 875us The test result is 800us does not meet the specification.

Test Item	Verify the TPS2640 tCB(dly) time when I(CB) < ILOAD < IFASTRIP.

Test method 1:	24V input voltage, $R_{(ILIM)}$=12.1K, use an electronic load apply 1A, and measure the tCB(dly).

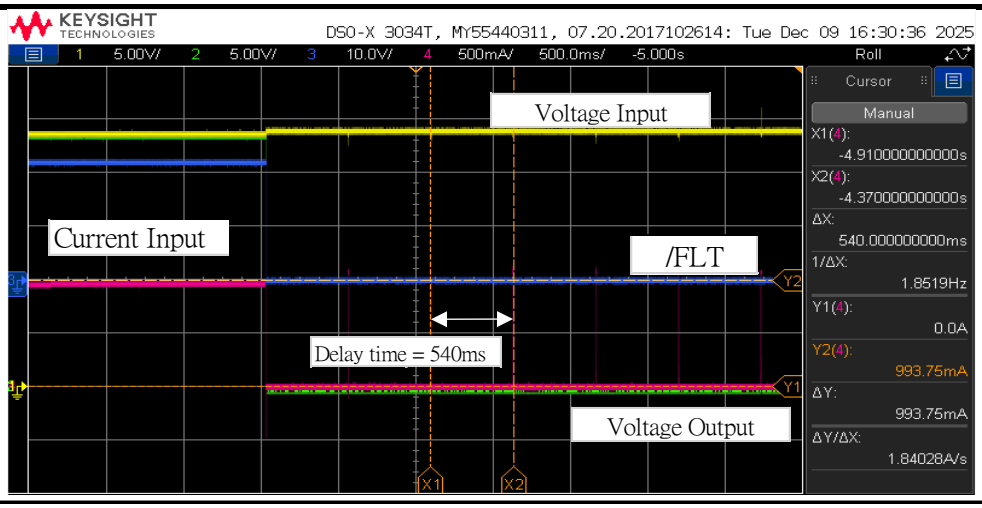


Spec					
	$t_{CB(dly)}$	FLT assertion delay in circuit breaker mode	MODE = OPEN, delay from $I_{(OUT)} > I_{(OL)}$ to FLT↓	4	ms

Test summary:	tCB(dly) is = 4ms The measured result of 3.94ms matches the specification.

Test Item	Verify the TPS2640 Auto-Retry tCBretry(dly) time.

Test method 1:	24V input voltage, $R_{(ILIM)}$=12.1K, use an electronic load apply 1A, and measure the tCBretry(dly).

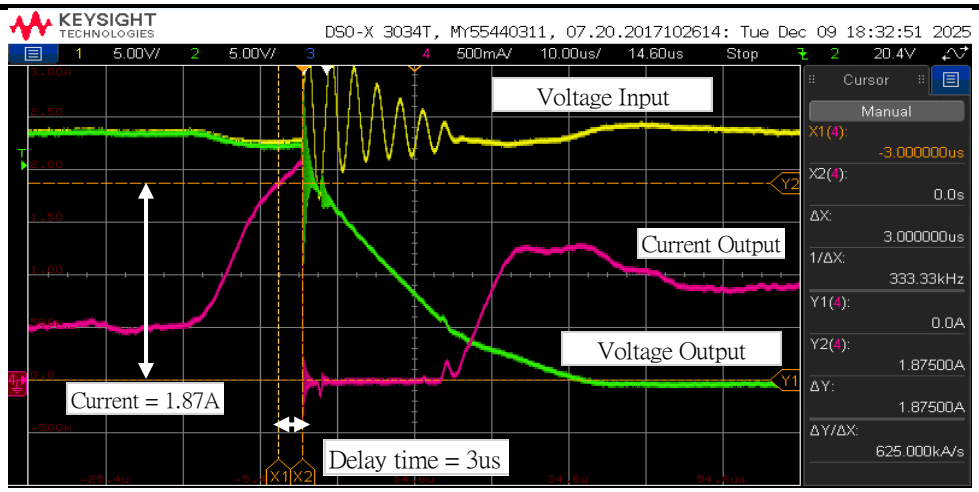


Spec					
	$t_{CBretry(dly)}$	Retry delay in circuit breaker mode	MODE = OPEN	540	ms

Test summary:	tCBretry(dly) is = 540ms The measured result of 540ms matches the specification.

Test Item	Verify the fast-trip delay time of the TPS2640.

Test method 1:	24V input voltage and I(FASTRIP) = 1.87 A, use an electronic load to increase the load from 0.5 A to 2 A, and measure the fast-trip trigger delay time.



Spec	CURRENT LIMIT				
	$t_{FASTTRIP(dly)}$	Fast-trip comparator delay	$I_{(OUT)} > I_{(FASTRIP)}$	250	ns

Test summary:	tFASTTRIP(dly) is = 250ns The test result is 3us does not meet the specification.