TPS274160x 40-V, 160-mΩ Quad-Channel Industrial Smart High-Side Switch

1 Features

- Quad-channel 160-mΩ smart high-side switch
- Channels can be paralleled for flexible operation
- Accurate adjustable current limiting (250mA to 4A)
  - ±15% accuracy at ≥ 500 mA
- 5 V - 36 V operating voltage range
- 48 V absolute maximum voltage
- Intelligent diagnostic features
  - TPS274160A: Open-drain fault output
  - TPS274160B: Analog current sense
  - Open-load and short to supply detection
- Robust protection features
  - Short-circuit protection
  - Inductive load flyback clamp
  - Undervoltage lockout (UVLO) protection
  - Loss of GND protection

2 Applications

- Digital output modules
- Standalone remote I/O
- Motor drives
- Building automation systems

3 Description

The TPS274160 is an industrial smart high-side switch with four integrated 160-mΩ NMOS power FETs. The device offers robust protection and full diagnostics to drive off-board inductive, capacitive, or resistive loads. The device enables flexible, multi-channel output configurations through paralleling channels and is in a very small WQFN package to enable usage in space constrained applications.

The device is protected against short circuit events and over-temperature events, safely shutting off the output during fault events. An external adjustable current limit improves the reliability of the system by actively limiting inrush or overload current, ensuring that the output current does not impact the supply rail and cause system brownouts or other failures.

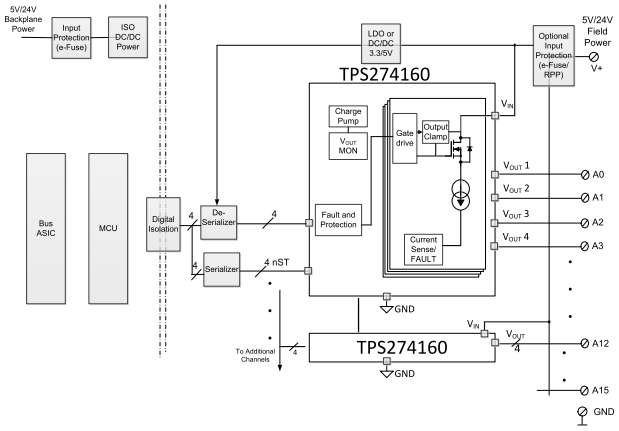
The device also integrates diagnostic features like output current monitoring and open load detection to allow for improved intelligence in modules and enable predictive maintenance functionality. Accurate current measurement or fault notification ensures systems, depending on the device variant, give the ability for systems to quickly diagnose and fix any module failures.

Device Information(1)

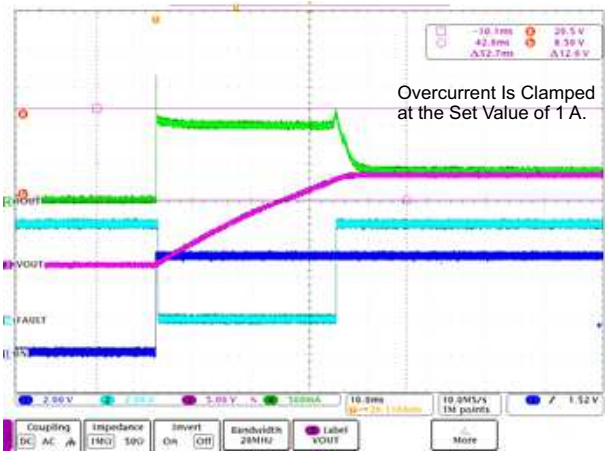
PART NUMBER	PACKAGE	BODY SIZE
TPS274160A	WQFN (28)	4 mm x 5 mm
TPS274160B		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Example



Driving a Capacitive Load With Adjustable Current Limit



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4 Revision History

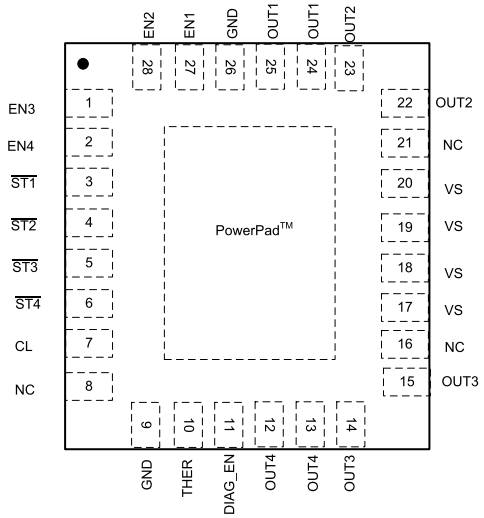
DATE	REVISION	NOTES
May 2020	*	Advance Information release

5 Device Comparison Table

PART NO.	FAULT REPORTING MODE
TPS274160**A**	Open-drain digital output
TPS274160**B**	Current-sense analog output

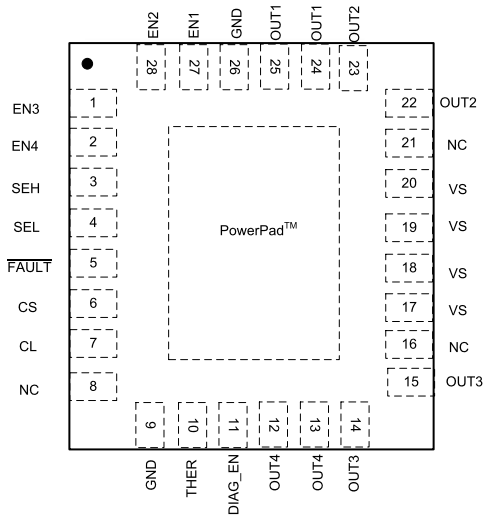
6 Pin Configuration and Functions

RLH Package
28-Pin WQFN With Exposed Thermal Pad
TPS274160A Top View



NC – No internal connection

RLH Package
28-Pin WQFN With Exposed Thermal Pad
TPS274160B Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
CL	7	7	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	—	6	O	Current-sense output
DIAG_EN	11	11	I	Enable-disable pin for diagnostics; internal pulldown
$\overline{\text{FAULT}}$	—	5	O	Global fault report with open-drain structure, ORed logic for quad-channel fault conditions
GND	9,26	9, 26	—	Ground pin
EN1	27	27	I	Input control for channel 1 activation; internal pulldown
EN2	28	28	I	Input control for channel 2 activation; internal pulldown
EN3	1	1	I	Input control for channel 3 activation; internal pulldown
EN4	2	2	I	Input control for channel 4 activation; internal pulldown
NC	8, 21, 16	8, 21, 16	—	No internal connection
$\overline{\text{ST1}}$	3	—	O	Open-drain diagnostic status output for channel 1
$\overline{\text{ST2}}$	4	—	O	Open-drain diagnostic status output for channel 2
$\overline{\text{ST3}}$	5	—	O	Open-drain diagnostic status output for channel 3
$\overline{\text{ST4}}$	6	—	O	Open-drain diagnostic status output for channel 4
SEH	—	3	I	CS channel-selection high bit; internal pulldown
SEL	—	4	I	CS channel-selection low bit; internal pulldown
THER	10	10	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
OUT1	24, 25	24, 25	O	Output of the channel 1 high side-switch, connected to the load
OUT2	22, 23	22, 23	O	Output of the channel 2 high side-switch, connected to the load
OUT3	14, 15	14, 15	O	Output of the channel 3 high side-switch, connected to the load

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Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
OUT4	12, 13	12, 13	O	Output of the channel 4 high side-switch, connected to the load
VS	17, 18, 19, 20	17, 18, 19, 20	I	Power supply
Thermal pad	—	—	—	Connect to device GND or leave floating

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply voltage(3)	Duration < 400 ms		48	V
Reverse polarity voltage(4)		–36		V
Current on GND pin	t < 2 minutes	–100	250	mA
Voltage on ENx, DIAG_EN, SEL, SEH, and THER pins		–0.3	7	V
Current on ENx, DIAG_EN, SEL, SEH, and THER pins		–10	—	mA
Voltage on $\overline{STx}$ or $\overline{FAULT}$ pins		–0.3	7	V
Current on $\overline{STx}$ or $\overline{FAULT}$ pins		–30	10	mA
Voltage on CS pin		–2.7	7	V
Current on CS pin		—	30	mA
Voltage on CL pin		–0.3	7	V
Current on CL pin		—	6	mA
Inductive load switch-off energy dissipation, single pulse, single channel(5)		—	TBD	mJ
Operating junction temperature		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Absolute maximum voltage, withstand 48-V load dump voltage for 400 ms.
(4) Reverse polarity condition:time t < 180s, reverse current < I_{rev2}, ENx = 0 V, GND pin 1-kΩ resistor in parallel with diode.
(5) Test condition: IL= 500 mA, T_J = 150°C.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD1)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except VS and VOUTx	±2000	V
$V_{(ESD2)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	VS and VOUTx with respect to GND	±5000	V
$V_{(ESD3)}$	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VS}	Supply operating voltage	5	36	V
	Voltage on ENx, DIAG EN, SEL, SEH, and THER pins	0	5	V
	Voltage on ST and FAULT pins	0	5	V
I_{nom}	Nominal DC load current per channel (all channels on)	0	1.35	A
T_A	Operating ambient temperature range	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS274160 RLH(QFN) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

(5 V < Vs < 36 V; −40°C < T_J < 125°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VS(uvr)}$	Undervoltage turnon	Vs rises up, Vs > Vs,uvr, device turns on.	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	Vs falls down, Vs < Vuvf, device shuts off.	3	3.2	3.4	V
$V_{VS(uv,hys)}$	Undervoltage shutdown, hysteresis			0.5		V
I_q	Device quiescent current no diagnostics	Vs < 30 V, ENx = 5 V, DIAG_EN = 0 V, Ioutx = 0 A, current limit = 2 A, all channels on,			8.0	mA
$t_{off(deg)}$	Standby mode deglitch time(1)	EN from high to low, if deglitch time > toff,deg, the device enters into standby mode.	10	12.5	15	ms
$I_{out(leak1)}$	Leakage current from OUT to GND in off-state	Vs = 24 V, ENx = DIAG_EN = OUTx = 0, measured on the GND pin			0.5	µA
$I_{out(leak2)}$	Output leakage current in off-state	Vs = 24 V, ENx = DIAG_EN = OUTx = 0, T_J = 25°C			0.5	µA
		Vs = 24 V, ENx = DIAG_EN = OUTx = 0, T_J = 125°C			3	µA
$r_{DS(on)}$	On-state resistance	Vs ≥ 5V, T_J = 25°C		160		mΩ
		Vs≥ 5 V, T_J = 125°C			260	mΩ
$I_{cl(int)}$	Internal current limit	Internal current limit value, CL pin connected to GND	8		14	A
$I_{cl(TSD)}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		6.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		70%		
$V_{ds(clamp\ )}$	Source-to-drain body diode voltage		50		70	V
V_F	Drain−source diode voltage	EN = 0, Iout = −0.15 A.	0.3	0.7	0.9	V
$I_{R(2)}$	Continuous reverse current from source to drain	t < 60 s, Vs = 24 V, ENx = 0 V, T_J = 25°C, single channel reversed current to supply		2.5		A
		t < 60 s, Vs = 24 V, ENx = 0 V, GND pin 1-kΩ resistor in parallel with diode. T_J = 25°C. Reverse-current condition, All channels reversed		2		A
V_{IH}	Logic high-level voltage		2			V
V_{IL}	Logic low-level voltage				0.8	V
$R_{(logic,pd)}$	Logic-pin pulldown resistor	DIAG_EN V_{VS} = V_{DIAG_EN}=5V	200	275	350	kΩ
$R_{(logic,pd)}$	Logic-pin pulldown resistor	ENx, SEL, SEH, THER pins, V_{VS} = V_{ENx}= V_{SEL}=V_{SEH}=V_{THER}=5V	100	175	250	kΩ
$I_{gnd(loss)}$	Output leakage current under GND loss condition				100	µA

(1) Value specified by design, not subject to production test

Electrical Characteristics (continued)

(5 V < Vs < 36 V; −40°C < T_J < 125°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ol(off)}$	Open load detection threshold	ENx = 0 V, when Vs – Voutx < Vol,off, duration longer than tol,off, then open load is detected, off state	1.6		2.6	V
$t_{ol(off)}$	Open-load detection threshold deglitch time	ENx =0V, when Vs – Voutx < Vol,off , duration longer than tol,off, then open load is detected, off state	300	560	800	µs
$V_{OL(STx)}$	Status low-output voltage	I_{STx} = 2 mA, version A only			0.2	V
$V_{OL(FAULT)}$	Fault low-output voltage	I_{FAULT} = 2 mA, version B only			0.2	V
$t_{cl(deg)}$	Deglitch time when current limit occurs(1)	ENx = DIAG_EN = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	80		180	µs
T_{SD}	Thermal shutdown threshold		160	175		°C
$T_{SD(rst)}$	Thermal shutdown status reset threshold			155		°C
T_{sw}	Thermal swing shutdown threshold			60		°C
T_{hys}	Hysteresis for resetting the thermal shutdown or thermal swing			10		°C
K_{CS}	Current sense ratio (Ver. B only)			300		
K_{CL}	Current limit ratio			2500		
$V_{CL(th)}$	Current limit internal threshold voltage(1)(2)			0.8		V
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	Vs = 24 V, Ioutx ≥ 5 mA (Version B)	-65		65	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	Vs = 24 V, Ioutx ≥ 25 mA (Version B)	-15		15	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	Vs = 24 V, Ioutx ≥ 50 mA (Version B)	-8		8	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	Vs = 24 V, Ioutx ≥ 100 mA (Version B)	-4		4	%
dK_{CS} / K_{CS}	Current sense accuracy, (I_{CS} × K_{CS} – I_{OUT}) /I_{OUT} × 100	Vs = 24 V, Ioutx ≥ 0.5 A (Version B)	-3		3	%
dK_{CL} / K_{CL}	External current limit accuracy, (I_{OUT} – I_{CL} × K_{CL} –) × 100 / I_{CL} × K_{CL}	Vs = 24 V, Ilimit ≥ 0.25 A	-20		20	%
dK_{CL} / K_{CL}	External current limit accuracy, (I_{OUT} – I_{CL} × K_{CL} –) × 100 / I_{CL} × K_{CL}	Vs = 24 V, 2 A ≤ Ilimit ≤ 7 A	-15		15	%
$V_{CS(lin)}$	Current-sense voltage linear range(1)	Vs ≥ 6.5 V	0		4	V
		5 V ≤ Vs < 6.5 V	0		Vs – 2.5	
$I_{OUTx(lin)}$	Output-current linear range(1)	Vs ≥ 6.5 V, Vcs,lin ≤ 4 V	0		2.5	A
		5 V ≤ Vs < 6.5 V, $V_{cs,lin}$ ≤ Vs – 2.5 V	0		2.5	
$V_{,CS(H)}$	Current sense pin output voltage	Vs ≥ 7 V, fault mode	4.5		6.5	V
		5 V ≤ Vs < 7 V, fault mode	Min(Vs-2, 4.5)		6.5	V
$I_{,CS(H)}$	Current-sense pin output current available in fault mode	Vcs = 4.5 V, Vs > 7 V	15			mA
$I_{CS(leak)}$	Current-sense leakage current in disabled mode	DIAG_EN = 0 V, TJ =125ºC			0.5	µA

(2) Vcl,th tolerance is included in the dK_{CL} / K_{CL} tolerance.

7.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d,on}$	Turnon delay time	Vs = 24V, DIAG_EN = 5 V, Ioutx = 0.5 A, IN rising edge to 10% of Voutx	20	50	90	µs
$t_{d,off}$	Turnoff delay time	Vs = 24V, DIAG_EN = 5 V, Ioutx = 0.5 A, IN falling edge to 90% of Voutx	20	50	90	µs
$t_{d,rise}$	Channel turnon time	V_S = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A 50% of EN to 90% of VOUT	90	120	150	µs
$t_{d,fall}$	Channel Turnoff time	V_S = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A 50% of EN to 10% of VOUT	90	120	150	µs

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Switching Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dV/dton	Turnon slew rate	Vs = 24V, DIAG_EN = 5 V, Ioutx = 0.5 A, Voutx from 10% to 90%	0.1	0.3	0.55	V/µs
dV/dtoff	Turnoff slew rate	Vs = 24V, DIAG_EN = 5 V, Ioutx = 0.5 A, Voutx from 90% to 10%	0.1	0.3	0.55	V/µs
$t_{d,match}$	$t_{d,rise} - t_{d,fall}$	Vs = 24V, Iload= 0.5A. $t_{d,\ rise}$ is the IN rising edge to Vout = 90%. $t_{d,\ fall}$ is the IN falling edge to Vout = 10%.	–50		50	µs
$t_{cs,off1}$	CS settling time from DIAG_EN disabled	Vs = 24 V, ENx = 5 V, Ioutx = 0.5 A. current limit = 2 A. DIAG_EN falling edge to 10% of Vcs.			20	µs
$t_{cs,on1}$	CS settling time from DIAG_EN enabled	Vs = 24 V, ENx = 5 V, Ioutx = 0.5 A. current limit is 2A. DIAG_EN rising edge to 90% of Vcs.			20	µs
$t_{cs,off2}$	CS settling time from IN falling edge	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A. current limit = 2 A. EN falling edge to 10% of Vcs			100	µs
$t_{cs,on2}$	CS settling time from IN rising edge	Vs = 24 V, DIAG_EN = 5 V, Ioutx = 0.5 A. current limit = 2 A. EN rising edge to 90% of Vcs			150	µs
t_{SEx}	Multi-sense transition delay from channel to channel	DIAG_EN=5V, current sense output delay when multi-sense pins SEL and SEH transition from channel to channel			50	µs

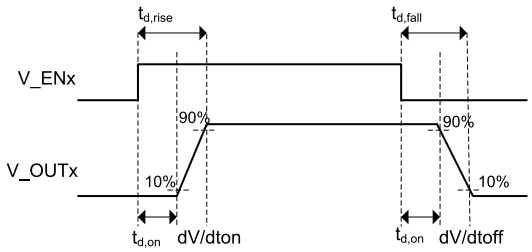


Figure 1. Output Delay Characteristics

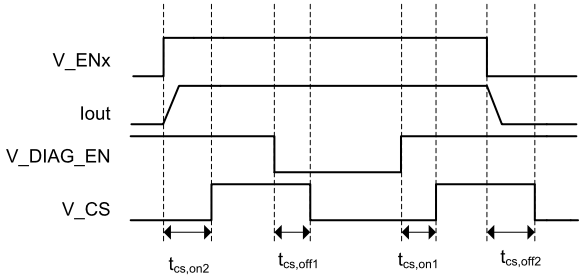


Figure 2. CS Delay Characteristics

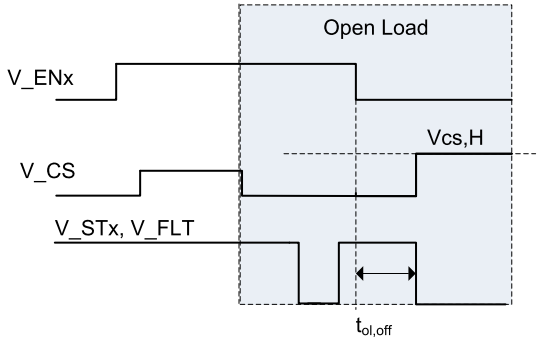


Figure 3. Open-Load Blanking-Time Characteristics

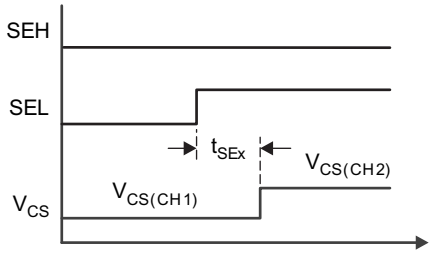


Figure 4. Multi-Sense Transition Delay

8 Detailed Description

8.1 Overview

The TPS274160 is an industrial smart high-side switch, with internal charge pump and quad-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls $\overline{STx}$ down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the $\overline{STx}$ pins together.

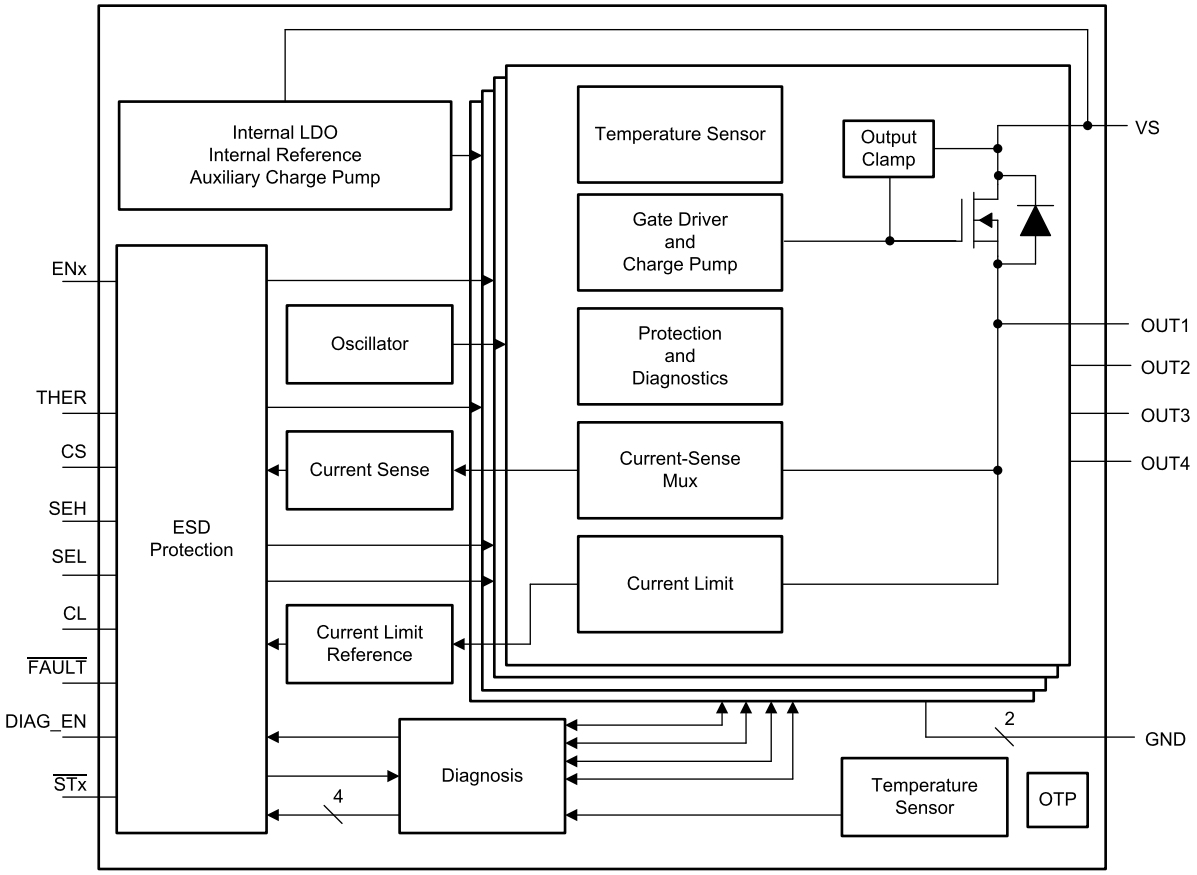
For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / $K_{(CS)}$ of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. $K_{(CS)}$ is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of $V_{CS(H)}$.

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS274160 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in Figure 5. All voltages are measured relative to the ground plane.

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Feature Description (continued)

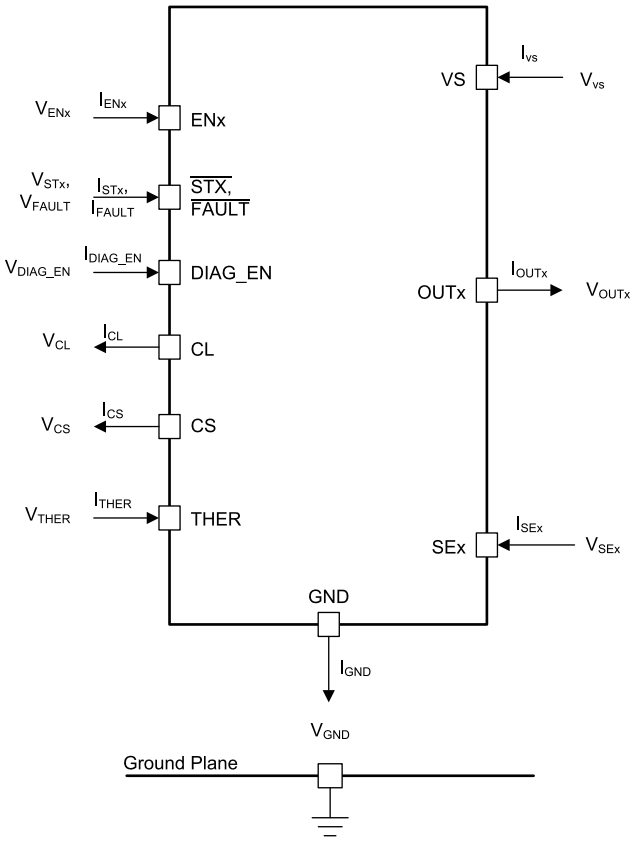

Figure 5. Voltage and Current Conventions

8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the version-B device. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

One integrated current mirror can source 1 / $K_{(CS)}$ of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the four channels. $K_{(CS)}$ is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See Figure 6 for more details.

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Feature Description (continued)

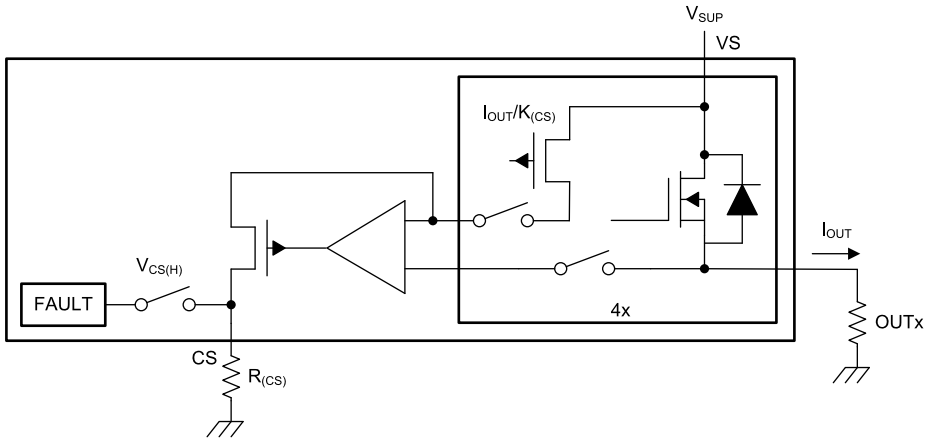

Figure 6. Current-Sense Block Diagram

When a fault occurs, the CS pin also works as a fault report with a pullup voltage, $V_{CS(H)}$. See Figure 7 for more details.

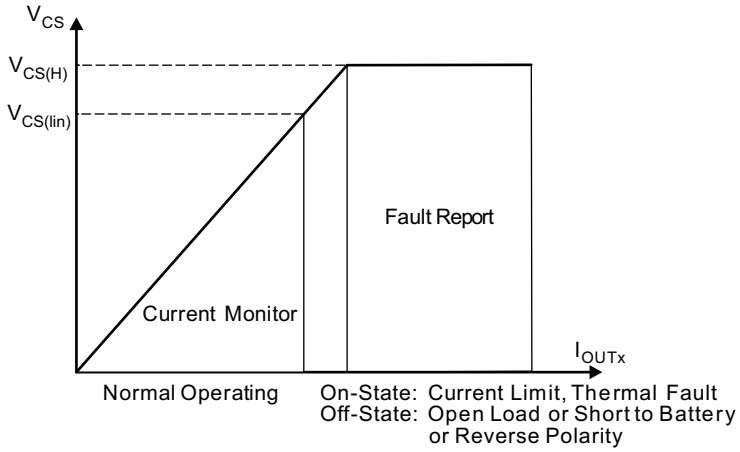

Figure 7. Current-Sense Output-Voltage Curve

Use Equation 1 to calculate $R_{(CS)}$.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \quad (1)$$

Take the following points into consideration when calculating $R_{(CS)}$.

- Ensure V_{CS} is within the current-sense linear region (V_{CS}, $I_{OUTx(lin)}$) across the full range of the load current. Check $R_{(CS)}$ with Equation 2.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS(lin)}}{I_{CS}} \quad (2)$$

- In fault mode, ensure I_{CS} is within the source capacity of the CS pin ($I_{CS(H)}$). Check $R_{(CS)}$ with Equation 3.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \quad (3)$$

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Feature Description (continued)

8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to $I_{CL(TSD)}$ to reduce the power dissipation on the power FET. See Figure 8 for more details.

The device has two current-limit thresholds.

- Internal current limit – The internal current limit is fixed at $I_{CL(int)}$. Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit – An external resistor is used to set the current-limit threshold. Use the Equation 4 to calculate the $R_{(CL)}$. $V_{CL(th)}$ is the internal band-gap voltage. $K_{(CL)}$ is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} \quad (4)$$

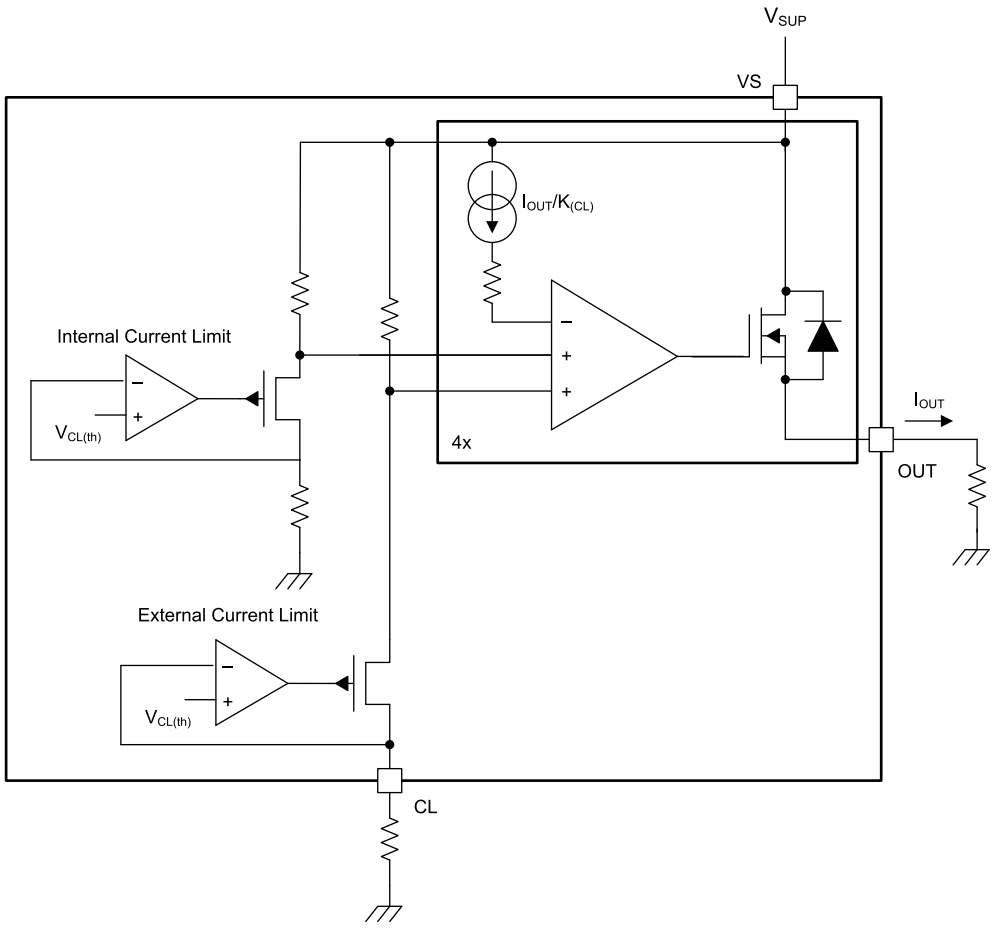

Figure 8. Current-Limit Block Diargam

ADVANCE INFORMATION

Feature Description (continued)

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the ENx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1 μs, typically. With this fast response, the device can achieve better inrush current-suppression performance.

8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely $V_{DS(clamp)}$.

$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (5)$$

During the period of demagnetization (t_{decay}), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ($E_{(VS)}$) and the energy of the load ($E_{(load)}$). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (6)$$

When an inductive load switches off, $E_{(HSS)}$ causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.

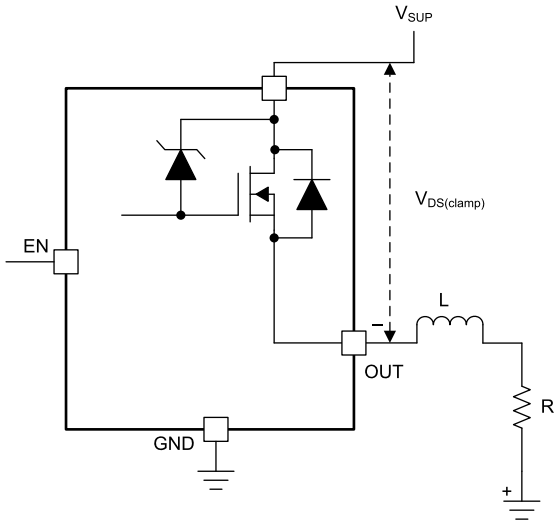

Figure 9. Drain-to-Source Clamping Structure

ADVANCE INFORMATION

Feature Description (continued)

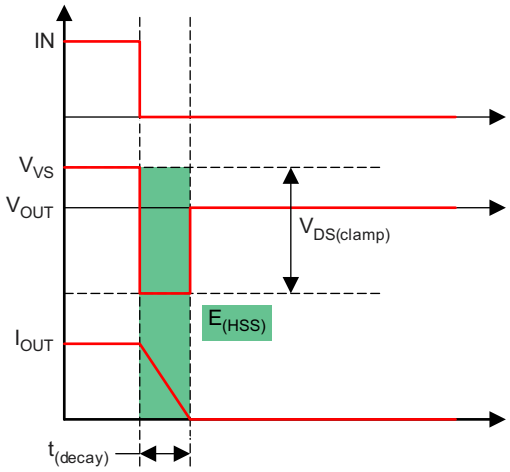

Figure 10. Inductive Load Switching-Off Diagram, note EN pin waveform referred to as IN

From the perspective of the high-side switch, $E_{(HSS)}$ equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t)\,dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)$$

$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[R \times I_{OUT(max)} - |V_{OUT}| \ln\left(\frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|}\right)\right] \quad (7)$$

When R approximately equals 0, $E_{(HSD)}$ can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I_{OUT(max)}^2 \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \quad (8)$$

Figure 11 is a waveform of the device driving an inductive load, and Figure 12 is waveform with an expanded time scale. Channel 1 is the EN signal (blue), channel 2 is the supply voltage V_{VS} (cyan), channel 3 is the output voltage V_{OUT} (magenta), channel 4 is the output current I_{OUT}(green), and channel M is the measured power dissipation $E_{(HSS)}$.

On the waveform, the duration of V_{OUT} from V_{VS} to (V_{VS} – $V_{DS(clamp)}$) is around 120 µs. The device also optimizes the switching-off slew rate when the clamp is active. This optimization can help the system design by keeping the effects of transient power and EMI to a minimum. As shown in Figure 11 and Figure 12, the controlled slew rate is around 0.5 V/µs.

ADVANCE INFORMATION

Feature Description (continued)

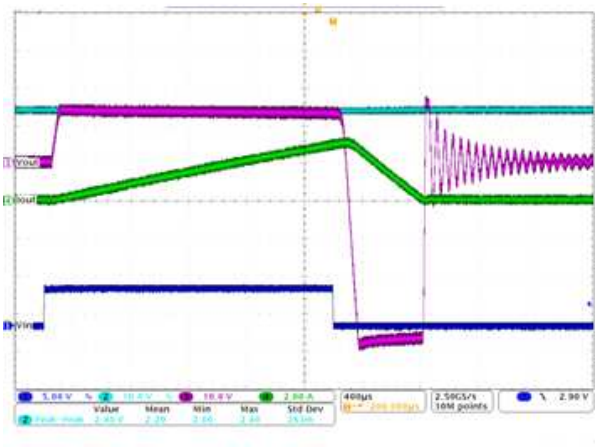

Figure 11. Inductive Load Switching-Off Waveform

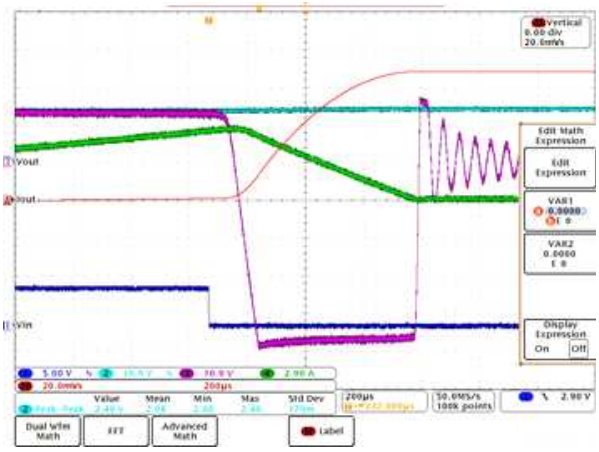

Figure 12. Inductive Load Switching-Off Expanded Waveform

Note that for PWM-controlled inductive loads, it is recommended to add the external freewheeling circuitry shown in Figure 13 to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See Figure 13 for more details.

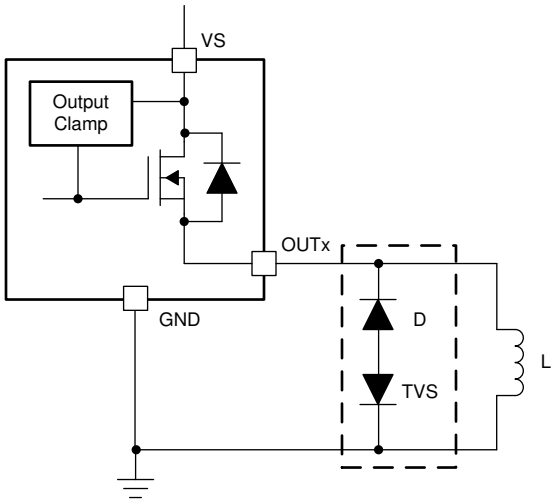

Figure 13. Protection With External Circuitry

8.3.5 Fault Detection and Reporting

8.3.5.1 Diagnostic Enable Function

The DIAG_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG_EN and ENx low.

8.3.5.2 Multiplexing of Current Sense

For version B, SEL and SEH are two pins to multiplex the shared current-sense function among the four channels. See Table 1 for more details.

ADVANCE INFORMATION

Feature Description (continued)

Table 1. Diagnosis Configuration Table

DIAG_EN	ENx	SEH	SEL	CS ACTIVATED CHANNEL	CS, $\overline{\text{FAULT}}$, $\overline{\text{STx}}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	—	High impedance	Diagnostics disabled, full protection
	L					Diagnostics disabled, no protection
H	—	0	0	Channel 1	See Table 2	See Table 2
		0	1	Channel 2		
		1	0	Channel 3		
		1	1	Channel 4		

8.3.5.3 Fault Table

Table 2 applies when the DIAG_EN pin is enabled.

Table 2. Fault Table

CONDITIONS	ENx	OUTx	THER	CRITERION	$\overline{\text{STx}}$ (VER. A)	CS (VER. B)	$\overline{\text{FAULT}}$ (VER. B)	FAULT RECOVERY
Normal	L	L	—	—	H	0	H	—
	H	H	—	—	H	In linear region	H	—
Overlaod, short to ground	H	L	—	Current limit triggered	L	$V_{CS(H)}$	L	Auto
Open load(1), short to supply, reverse polarity	L	H	—	$V_{VS} - V_{OUTx} < V_{(ol,off)}$	L	$V_{CS(H)}$	L	Auto
Thermal shutdown	H	—	L	T_{SD} triggered	L	$V_{CS(H)}$	L	Output auto-retry. Fault recovers when $T_J < T_{(SD,rst)}$ or when ENx toggles.
			H					Output latch off. Fault recovers when ENx toggles.
Thermal swing	H	—	—	T_{SW} triggered	L	$V_{CS(H)}$	L	Auto

(1) An external pullup is required for open-load detection.

8.3.5.4 $\overline{\text{STx}}$ and $\overline{\text{FAULT}}$ Reporting

For version A, four individual $\overline{\text{STx}}$ pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls $\overline{\text{STx}}$ down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the $\overline{\text{STx}}$ pins together.

For version B, a global $\overline{\text{FAULT}}$ pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the $\overline{\text{FAULT}}$ pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the $\overline{\text{FAULT}}$ report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, $V_{CS(H)}$.

8.3.6 Full Diagnostics

8.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is $I_{CL(TSD)}$ to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

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8.3.6.2 Open-Load Detection

8.3.6.2.1 Channel On

When a channel is on and an open-load event occurs, it can be detected as an ultra-low V_{CS} voltage at the CS pin and handled by the micro-controller. The high-accuracy current sense in the low current range, enables the open-load detection at very low current thresholds. Note that the detection is not reported on the $\overline{STx}$ or $\overline{FAULT}$ pins. The microcontroller must proactively multiplex the SEL and SEH pins to detect the channel-on open-load fault.

8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ($V_{VS} – V_{OUTx} < V_{(ol,off)}$), and the fault is reported out.

There is always a leakage current $I_{(ol,off)}$ present on the output due to internal logic control path or external humidity, corrosion, and so forth. Thus, TI recommends an external pullup resistor to offset the leakage current when an open load is detected. The recommended pullup resistance is 20 kΩ.

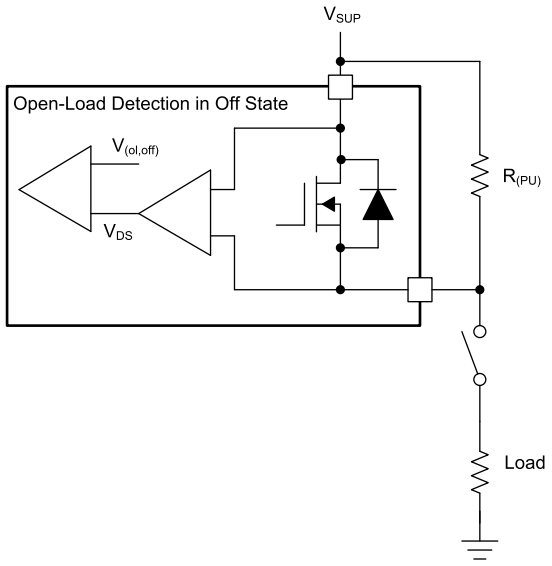


Figure 14. Open-Load Detection in Off-State

8.3.6.3 Short-to-Supply Detection

Short-to-supply has the same detection mechanism and behavior as open-load detection, in both the on-state and off-state. See Table 2 for more details.

In the on-state, reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state.

- If $V_{OUTx} – V_{VS} < V_{(F)}$ (body diode forward voltage), no reverse current occurs.
- If $V_{OUTx} – V_{VS} > V_{(F)}$, reverse current occurs. The current must be limited to less than $I_{R(1)}$. Setting an ENx pin high can minimize the power stress on its channel. Also, for external reverse protection, see Reverse-Current Protection for more details.

8.3.6.4 Input Reverse Polarity Detection

Reverse polarity detection has the same detection mechanism and behavior as open-load detection both in the on-state and off-state. See Table 2 for more details.

In the on-state, the reverse current flows through the FET instead of the body diode, leading to less power dissipation. Thus, the worst case occurs in the off-state. The reverse current must be limited to less than $I_{R(2)}$. Set the related ENx pin high to keep the power dissipation to a minimum. For external reverse-blocking circuitry, see Reverse-Current Protection for more details.

ADVANCE INFORMATION

8.3.6.5 Thermal Fault Detection

To protect the device in severe power stressing cases, the device implements two types of thermal fault detection, absolute temperature protection (thermal shutdown) and dynamic temperature protection (thermal swing). Respective temperature sensors are integrated close to each power FET, so the thermal fault is reported by each channel. This arrangement can help the device keep the cross-channel effect to a minimum when some channels are in a thermal fault condition.

8.3.6.5.1 Thermal Shutdown

Thermal shutdown is active when the absolute temperature $T_J > T_{(SD)}$. When thefrmal shutdown occurs, the respective output turns off. The THER pin is used to configure the behavior after the thermal shutdown occurs.

- When the THER pin is low, thermal shutdown operates in the auto-retry mode. The output automatically recovers when $T_J < T_{(SD)} – T_{(hys)}$, but the current is limited to $I_{CL(TSD)}$ to avoid repetitive thermal shutdown. The thermal shutdown fault signal is cleared when $T_J < T_{(SD,rst)}$ or after toggling the related ENx pin.
- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related ENx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when $\Delta T = T_{(FET)} – T_{(Logic)} > T_{(sw)}$, then the output turns off. The output automatically recovers and the fault signal clears when $\Delta T = T_{(FET)} – T_{(Logic)} < T_{(sw)} – T_{(hys)}$. Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 15, multiple thermal swings are triggered before thermal shutdown occurs.

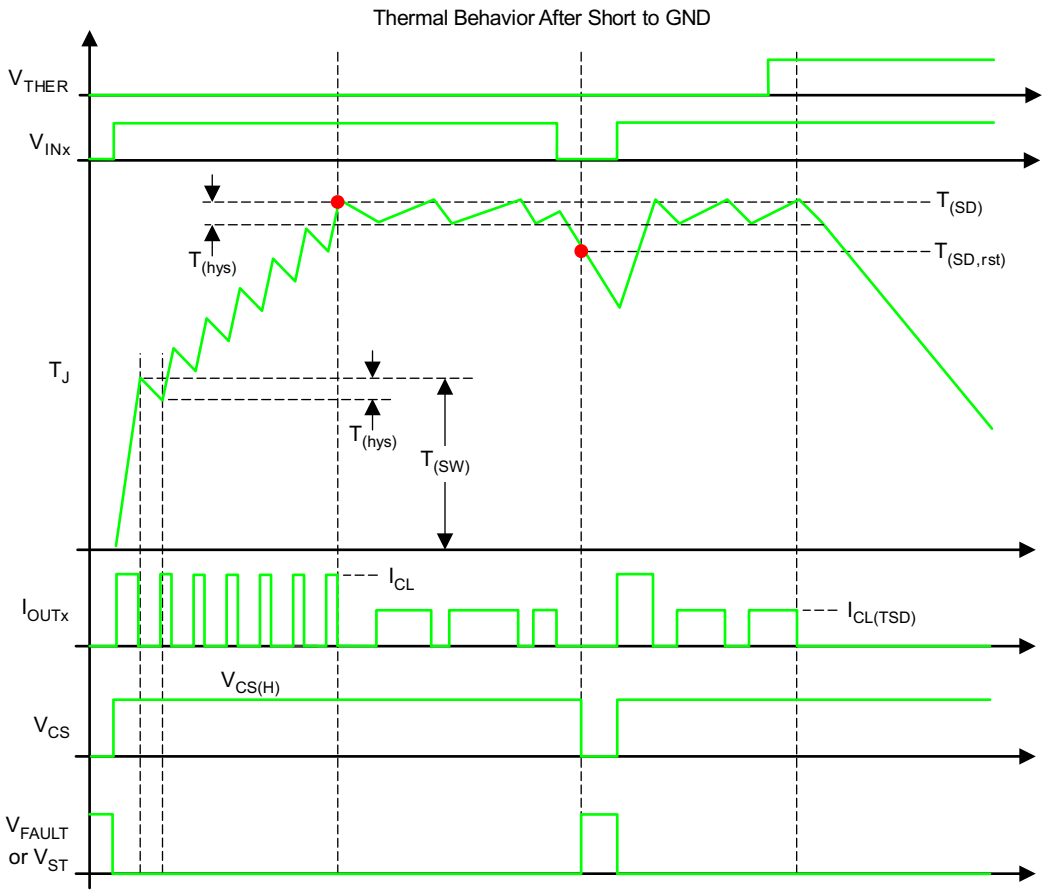


Figure 15. Thermal Behavior Diagram

8.3.7 Full Protections

8.3.7.1 UVLO Protection

The device monitors the supply voltage V_{VS}, to prevent unpredicted behaviors when V_{VS} is too low. When V_{VS} falls down to $V_{VS(uvf)}$, the device shuts down. When V_{VS} rises up to $V_{VS(uvr)}$, the device turns on.

8.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the ENx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

8.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the ENx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pinss to maintain the inductance current. To protect the system in this condition, TI recommends two types of external protections: the GND network or the external free-wheeling diode.

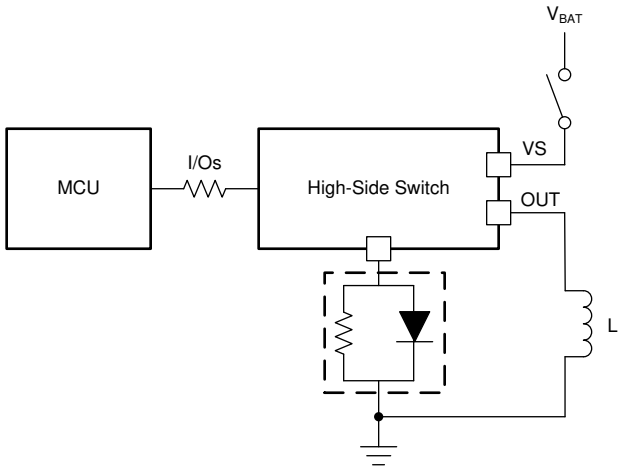


Figure 16. Protection for Loss of Power Supply, Method 1

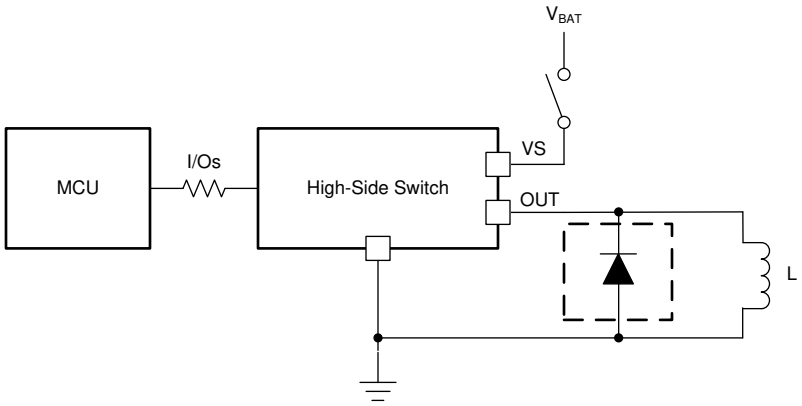


Figure 17. Protection for Loss of Power Supply, Method 2

8.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to supply and reverse polarity.

- When a short to the supply occurs, there is only reverse current through the body diode. $I_{R(1)}$ specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin. $I_{R(2)}$ specifies the limit of the reverse current.

ADVANCE INFORMATION

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.

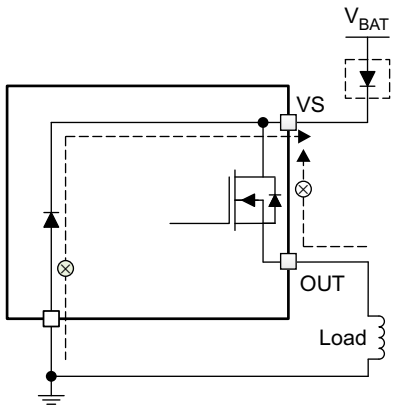


Figure 18. Reverse-Current External Protection, Method 1

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-kΩ resistor in parallel with an >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.

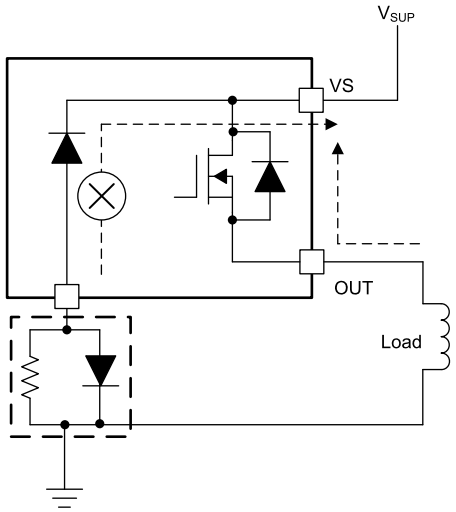


Figure 19. Reverse-Current External Protection, Method 2

8.3.7.5 MCU I/O Protection

In some severe conditions, such as the high voltage transients or the loss of supply with inductive loads, a negative pulse occurs on the GND pin This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-kΩ when using a 3.3-V microcontroller and 10-kΩ for a 5-V microcontroller.

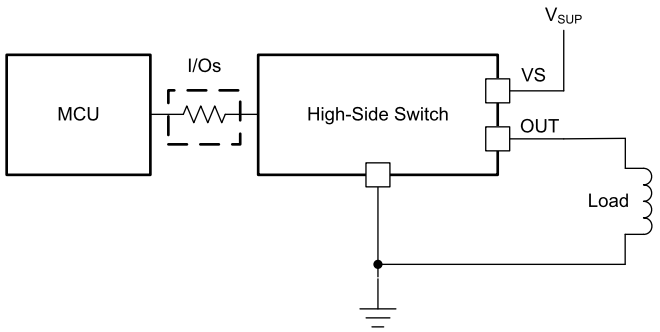


Figure 20. MCU I/O External Protection

8.4 Device Functional Modes

8.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for $t > t_{(off,deg)}$ to enter the standby mode, where $t_{(off,deg)}$ is the standby mode deglitch time used to avoid false triggering. Figure 21 shows a working-mode diagram.

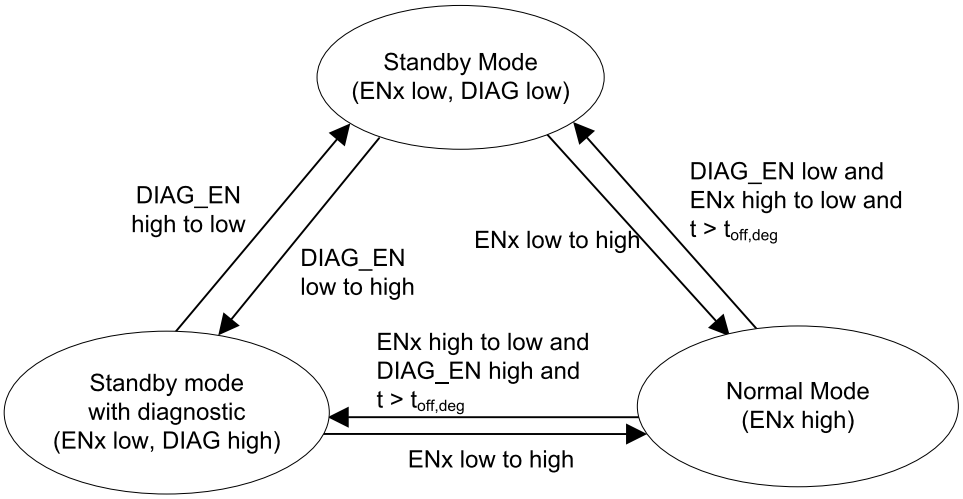


Figure 21. Working Modes

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS274160 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including common industrial loads like low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

9.2 Typical Application

The following figure shows an example of the external circuitry connections based on the version-B device.

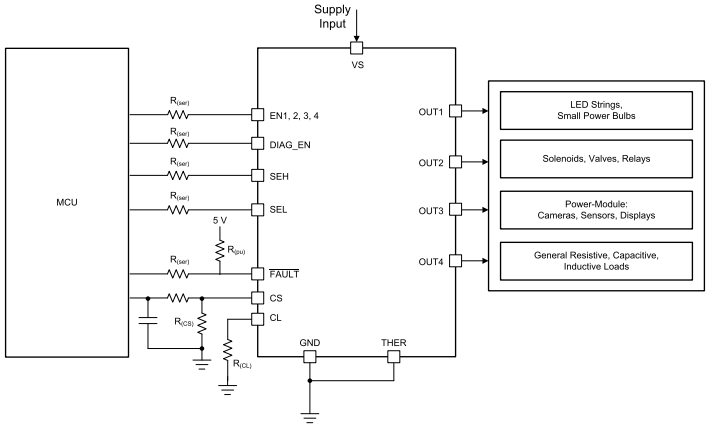


Figure 22. Typical Application Diagram.

9.2.1 Design Requirements

- V_{VS} = 24 V nominal
- Load range is from 0.1 A to 1 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 2.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU

9.2.2 Detailed Design Procedure

To keep the 1-A nominal current in the 0 to 4-V current-sense range, calculate the $R_{(CS)}$ resistor using Equation 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 300}{1} = 1200\ \Omega \quad (9)$$

To set the adjustable current limit value at 2.5-A, calculate $R_{(CL)}$ using Equation 10.

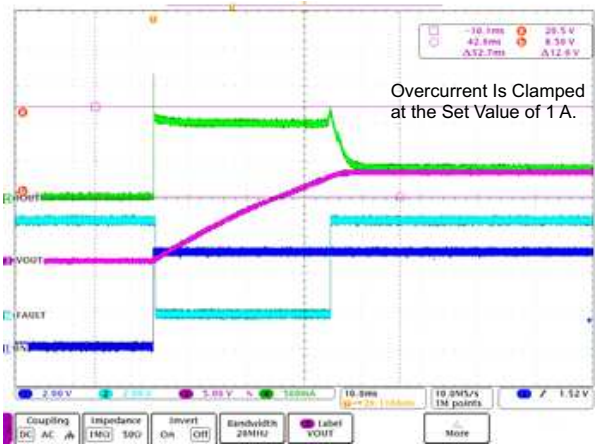
$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 2500}{2.5} = 800\ \Omega \quad (10)$$

TI recommends $R_{(ser)}$ = 10 kΩ for 5-V MCU, and $R_{(pu)}$ = 10 kΩ as the pullup resistor.

Typical Application (continued)

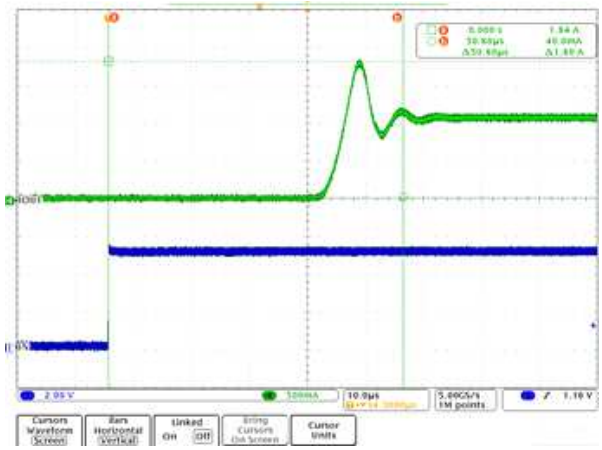
9.2.3 Application Curves

Figure 23 shows a test example of soft-start when driving a big capacitive load. Figure 24 shows an expanded waveform of the output current.



V_S = 12 V
Load current = 0.4 A
CH2 = $\overline{FAULT}$
ENx = ↑
C_L = 2.3 mF
CH3 = output voltage
Current limit = 1 A
CH1 = ENx
CH4 = output current

Figure 23. Driving a Capacitive Load With Adjustable Current Limit



V_{VS} = 12 V
Load current = 0.4 A
CH2 = $\overline{FAULT}$
ENx = ↑
C_L = 2.3 mF
CH3 = output voltage
Current limit = 1 A
CH1 = ENx
CH4 = output current

Figure 24. Driving a Capacitive Load, Expanded Waveform

10 Power Supply Recommendations

The device is qualified for industrial applications. The normal power supply connection is a 24-V industrial system. The supply voltage should be within the range specified in the *Recommended Operating Conditions*.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

To prevent thermal shutdown, T_J must be less than 150°C. The WQFN package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

11.2 Layout Examples

11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

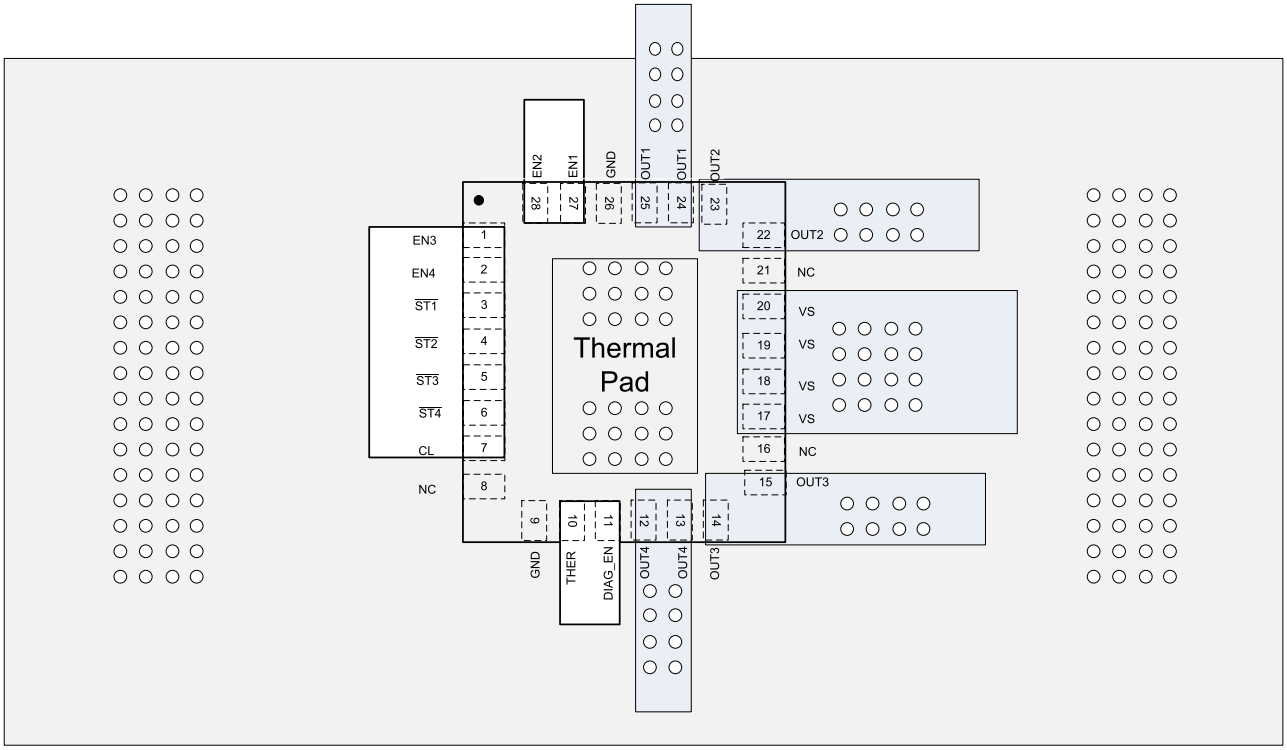


Figure 25. Layout Example Without a GND Network

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
PTPS274160ARLHR	PREVIEW	WQFN	RLH	28	3000	TBD	NiPdAuCu	LEVEL2-260C-1 Year	-40 to 125	274160A
PTPS274160BRLHR	PREVIEW	WQFN	RLH	28	3000	TBD	NiPdAuCu	LEVEL2-260C-1 Year	-40 to 125	274160B

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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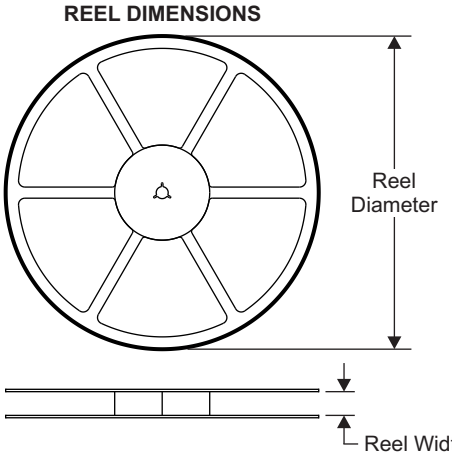
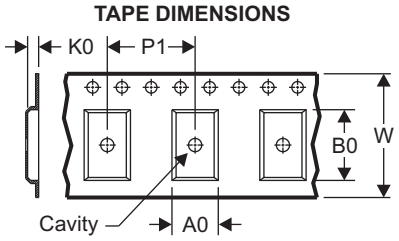
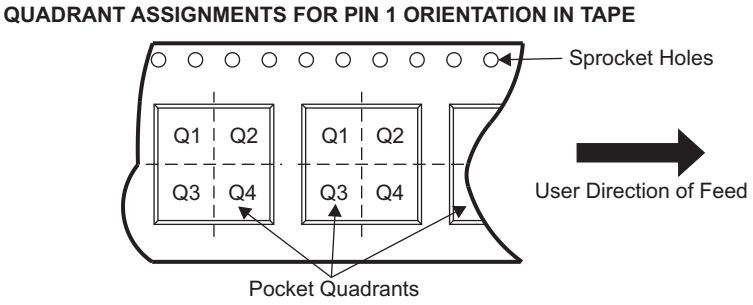
ADVANCE INFORMATION

13.1.2 Tape and Reel Information





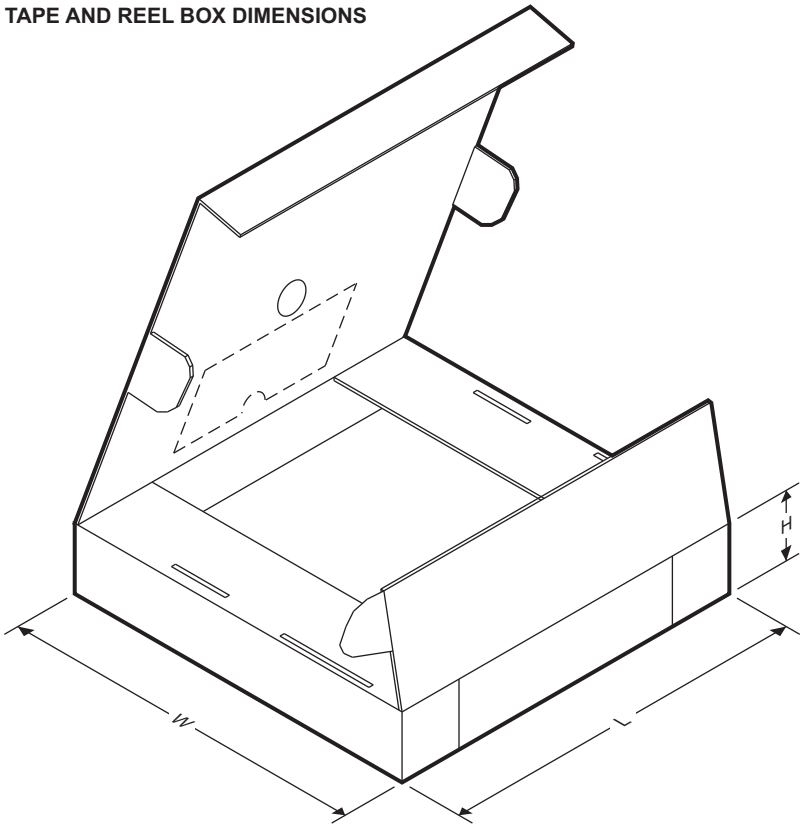
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTP274160ARLHR	WQFN	RLH	28	3000	330	12	4.3	5.3	1.3	8	12.4	Q1
PTP274160BRLHR	WQFN	RLH	28	3000	330	12	4.3	5.3	1.3	8	12.4	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTP274160ARLHR	WQFN	RLH	28	3000	367	367	35
PTP274160BRLHR	WQFN	RLH	28	3000	367	367	35

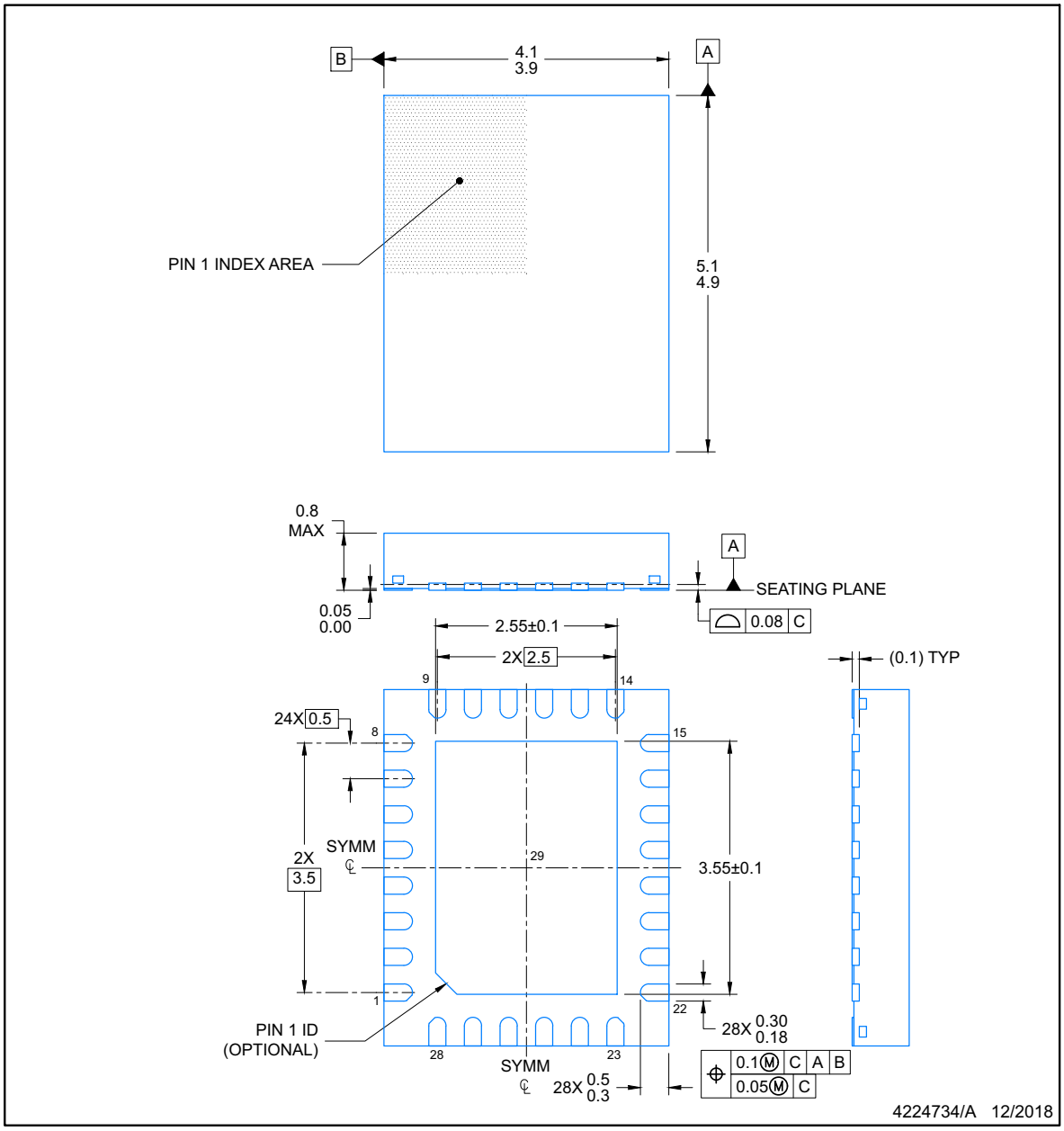
ADVANCE INFORMATION

PACKAGE OUTLINE

RLH0028A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

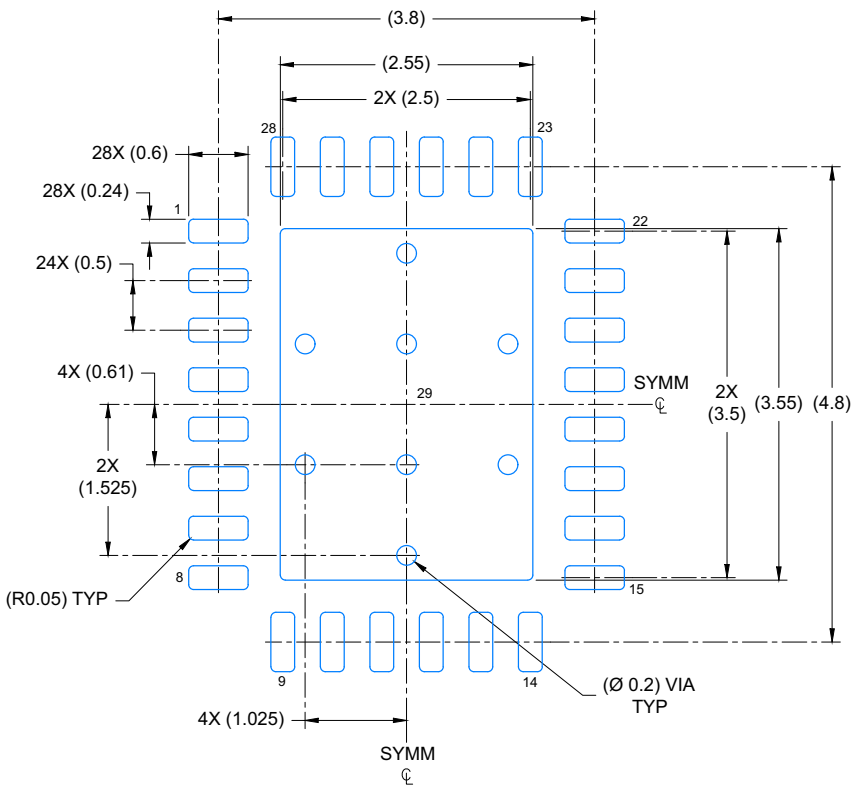
ADVANCE INFORMATION

ADVANCE INFORMATION

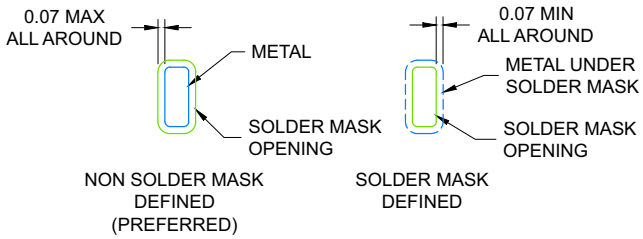
EXAMPLE BOARD LAYOUT

RLH0028A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

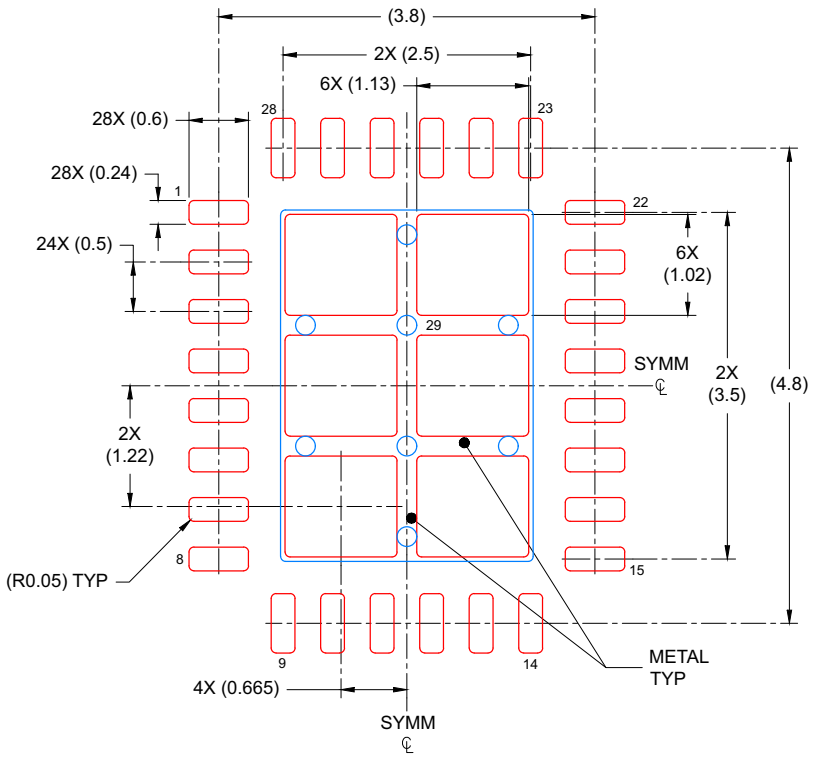
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RLH0028A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS274160ARLHR	ACTIVE	WQFN	RLH	28	3000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS274160BRLHR	ACTIVE	WQFN	RLH	28	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TPS274160ARLHR	PREVIEW	WQFN	RLH	28	3000	TBD	Call TI	Call TI	-40 to 125		
TPS274160BRLHR	PREVIEW	WQFN	RLH	28	3000	TBD	Call TI	Call TI	-40 to 125		

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OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

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