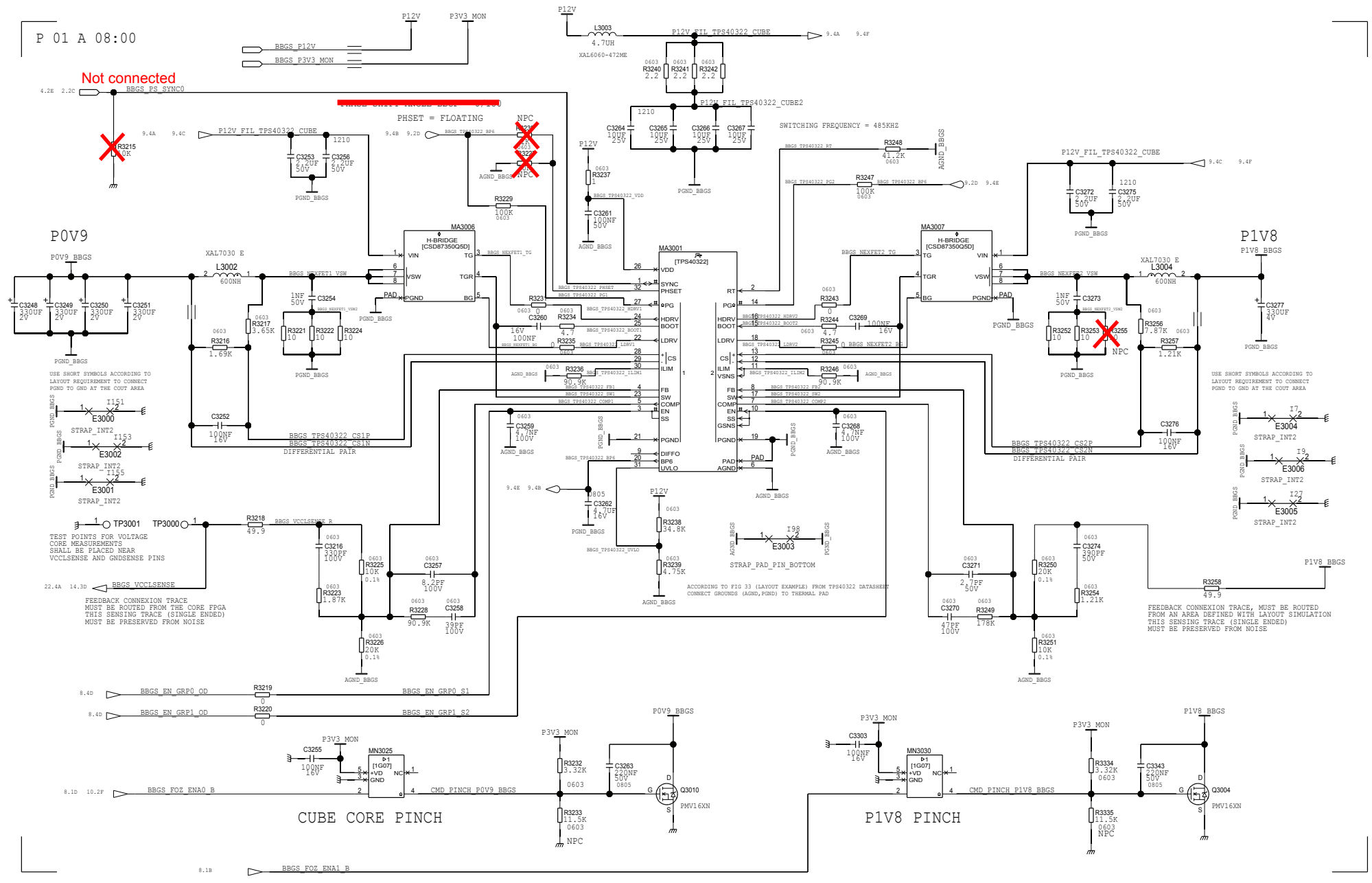


P 01 A 08:00

Not connected



USE SHORT SYMBOLS ACCORDING TO LAYOUT REQUIREMENT TO CORRECT PGND TO GND AT THE COUT AREA

ESTRIP_BBSGS
STRAP_INT2
E3000
E3002
STRAP_INT2
E3001
STRAP_INT2

TEST POINTS FOR VOLTAGE CORE MEASUREMENTS SHALL BE PLACED NEAR VCCLSNSE AND GNDSENSE PINS

TP3001 TP3000

FEEDBACK CONNEXION TRACE MUST BE ROUTED FROM THE CORE FPGA THIS SENSING TRACE (SINGLE ENDED) MUST BE PRESERVED FROM NOISE

BBGS_EN_GRP0_OD
BBGS_EN_GRP1_OD

BBGS_FOZ_ENA0_B

BBGS_FOZ_ENA1_B

CUBE CORE PINCH

P18V PINCH

USE SHORT SYMBOLS ACCORDING TO LAYOUT REQUIREMENT TO CORRECT PGND TO GND AT THE COUT AREA

STRAP_INT2
E3004
STRAP_INT2
E3006
STRAP_INT2
E3005
STRAP_INT2

FEEDBACK CONNEXION TRACE, MUST BE ROUTED FROM AN AREA DEFINED WITH LAYOUT SIMULATION THIS SENSING TRACE (SINGLE ENDED) MUST BE PRESERVED FROM NOISE

P18V_BBSGS

P18V_BBSGS

P18V_BBSGS

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4
 3
 2
 1