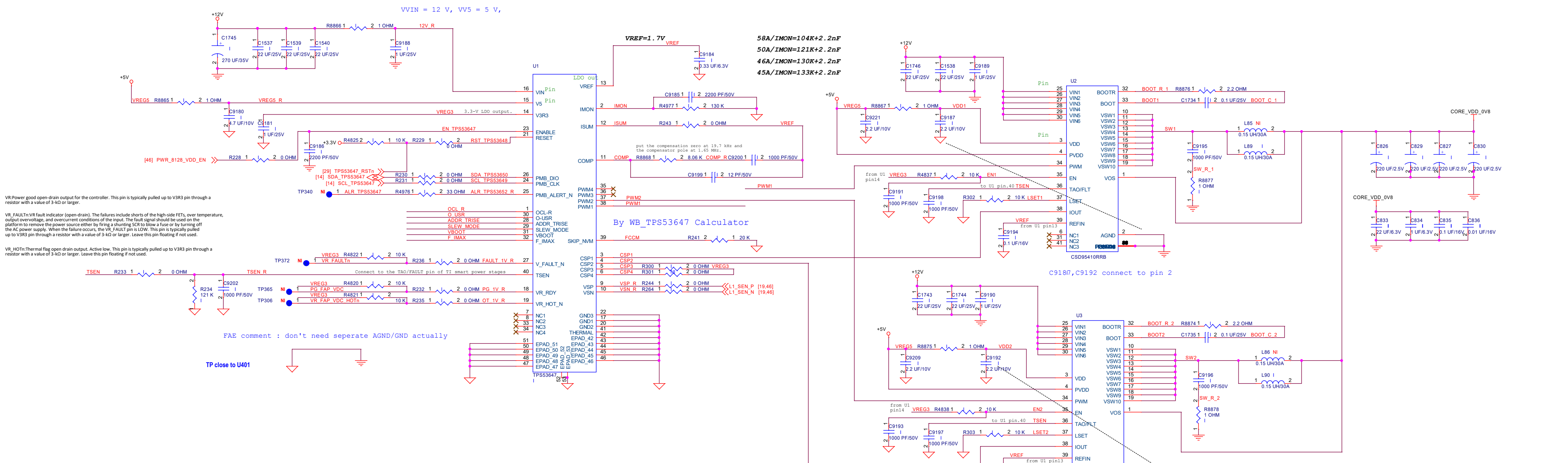
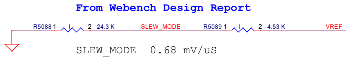


VVIN = 12 V, VV5 = 5 V,
VREF=1.7V
58A/IMON=104K+2.2nF
50A/IMON=121K+2.2nF
46A/IMON=130K+2.2nF
45A/IMON=133K+2.2nF
U1
TPS53647
U2
CSD95410RRB
U3
CSD95410RRB
CORE_VDD_0V8
By WB_TPS53647 Calculator
put the compensation zero at 19.7 kHz and the compensator pole at 1.65 MHz.
Connect to the TAO/FAULT pin of TI smart power stages
FAE comment : don't need seperate AGND/GND actually
TP close to U401
C9187,C9192 connect to pin 2
VR:Power good open-drain output for the controller. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger.
VR_FAULTn:VR fault indicator (open-drain). The failures include shorts of the high-side FETs, over temperature, output overvoltage, and overcurrent conditions of the input. The fault signal should be used on the platform to remove the power source either by firing a shunting SCR to blow a fuse or by turning off the AC power supply. When the failure occurs, the VR_FAULT pin is LOW. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger. Leave this pin floating if not used.
VR_HOTn:Thermal flag open drain output. Active low. This pin is typically pulled up to V3R3 pin through a resistor with a value of 3-kΩ or larger. Leave this pin floating if not used.

VBOOT:Voltage divider to VREF pin. A resistor (RVBOOT) connected between this pin and GND sets 3 bits (B[3:1]). The voltage level (VvBOOT) sets 4 bits (B[7:4]). The total 7 bits set 7 of 8 bits of VID of boot voltage (B[7:1]). The device latches these settings when V3R3 powers up.

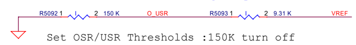
1.CSD95410RRB VOS connect to output side of Inductor
2.Correct Pin 32/Pin 33 external RC position
3.Connect TPS53647 pin V5 & CSD95410RRB pin VDD/PVDD to external power 5V
4.Connect CSD95410RRB pin 39 to TPS53647 的Pin 13(VREF)
5. C9181 接 AGND
6. Change C9191/C9193 to IC pin for low pass scheme.
7. Correct PWM1/PWM2 to U1 pin

From Webench Design Report



SLEW_MODE 0.68 mV/uS

From Webench Design Report

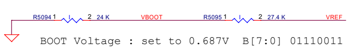


Set OSR/USR Thresholds :150K turn off

$R_{O\text{-}USR}$ (kΩ)	OSR THRESHOLD (mV)
20	30
24	40
30	60
39	80
56	100
75	120
100	140
150	OFF

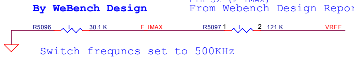
From Webench Design Report

VBOOT=1.7V*[24K/(24K+27.4K)} = 0.793V VREF=1.7V



BOOT Voltage : set to 0.687V B[7:0] 01110011

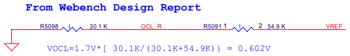
By WeBench Design Pin 32 (F-IMAX) **From Webench Design Report**



Switch frequncs set to 500KHz

R_{BOOT} (kΩ)	BOOT VOLTAGE VID $B_3B_2B_1$
20	000
24	001
30	010
39	011
56	100
75	101
100	110
150	111

From Webench Design Report



VOCL=1.7V*[30.1K/(30.1K+54.9K)} = 0.602V

Per-Phase Valley Current Limit And Ramp Level set to 30A

Table 79. Boot Voltage VID Selection (Step 2)

V_{VBOOT} (V)	BOOT VOLTAGE VID $B_7B_6B_5B_4$
$V_{VBOOT} \leq 0.053V \pm 20$ mV	0000
$V_{VBOOT} = 0.159V \pm 20$ mV	0001
$V_{VBOOT} = 0.226V \pm 20$ mV	0010
$V_{VBOOT} = 0.372V \pm 20$ mV	0011
$V_{VBOOT} = 0.478V \pm 20$ mV	0100
$V_{VBOOT} = 0.584V \pm 20$ mV	0101
$V_{VBOOT} = 0.691V \pm 20$ mV	0110
$V_{VBOOT} = 0.797V \pm 20$ mV	0111
$V_{VBOOT} = 0.903V \pm 20$ mV	1000
$V_{VBOOT} = 1.009V \pm 20$ mV	1001
$V_{VBOOT} = 1.116V \pm 20$ mV	1010
$V_{VBOOT} = 1.222V \pm 20$ mV	1011
$V_{VBOOT} = 1.328V \pm 20$ mV	1100
$V_{VBOOT} = 1.434V \pm 20$ mV	1101
$V_{VBOOT} = 1.541V \pm 20$ mV	1110
$V_{VBOOT} = 1.615V \pm 10$ mV	1111

Table 80. Boot Voltage VID Selection (Step 3)

R_{ADDR} (kΩ)	BOOT VOLTAGE VID B_0
20 or 30 or 56 or 100	0
24 or 39 or 75 or 150	1

V_{OCL}(V)	$R_{OCL\text{-}R}$ (kΩ)	PER-PHASE VALLEY CURRENT LIMIT (A)
≤ 0.85	20	24
	24	27
	30	30
	39	33
	56	36
	75	39
	100	42
	150	45
≥ 0.95	20	48
	24	51
	30	54
	39	57
	56	60
	75	63
	100	66
	150	69

R5086 = 24K /R5087 = 16.5K => 1.007V / 0x71h

VREF=1.7V

0.053V +/- 0.02V = 0.073V ~ 0.033V

PMBus address bits set ($11P_40P_2P_1P_0$)	$V_{ADDR\text{-}TRISE} \leq 0.053$ V with ±20 mV tolerance	1100000
	$V_{ADDR\text{-}TRISE} = 0.159$ V with ±20 mV tolerance	1100001
	$V_{ADDR\text{-}TRISE} = 0.266$ V with ±20 mV tolerance	1100010
	$V_{ADDR\text{-}TRISE} = 0.372$ V with ±20 mV tolerance	1100011
	$V_{ADDR\text{-}TRISE} = 0.478$ V with ±20 mV tolerance	1100100
	$V_{ADDR\text{-}TRISE} = 0.584$ V with ±20 mV tolerance	1100101
	$V_{ADDR\text{-}TRISE} = 0.691$ V with ±20 mV tolerance	1100110
	$V_{ADDR\text{-}TRISE} = 0.797$ V with ±20 mV tolerance	1100111
	$V_{ADDR\text{-}TRISE} = 0.903$ V with ±20 mV tolerance	1110000
	$V_{ADDR\text{-}TRISE} = 1.009$ V with ±20 mV tolerance	1110001
	$V_{ADDR\text{-}TRISE} = 1.116$ V with ±20 mV tolerance	1110010
	$V_{ADDR\text{-}TRISE} = 1.222$ V with ±20 mV tolerance	1110011
	$V_{ADDR\text{-}TRISE} = 1.328$ V with ±20 mV tolerance	1110100
	$V_{ADDR\text{-}TRISE} = 1.434$ V with ±20 mV tolerance	1110101
	$V_{ADDR\text{-}TRISE} = 1.541$ V with ±20 mV tolerance	1110110
	$V_{ADDR\text{-}TRISE} = 1.615$ V with ±10 mV tolerance	1110111