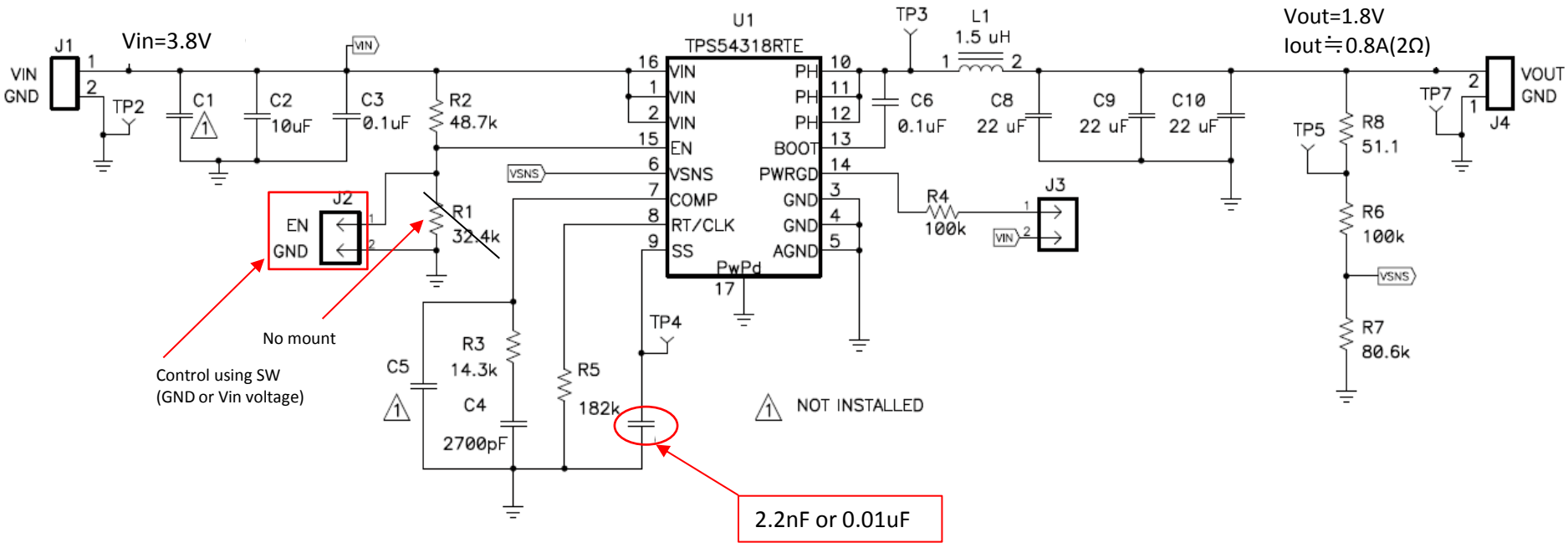
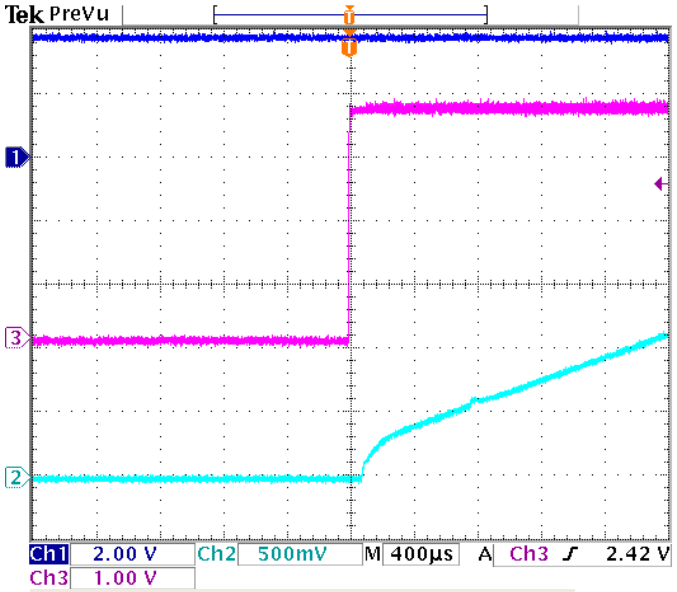
Test condition

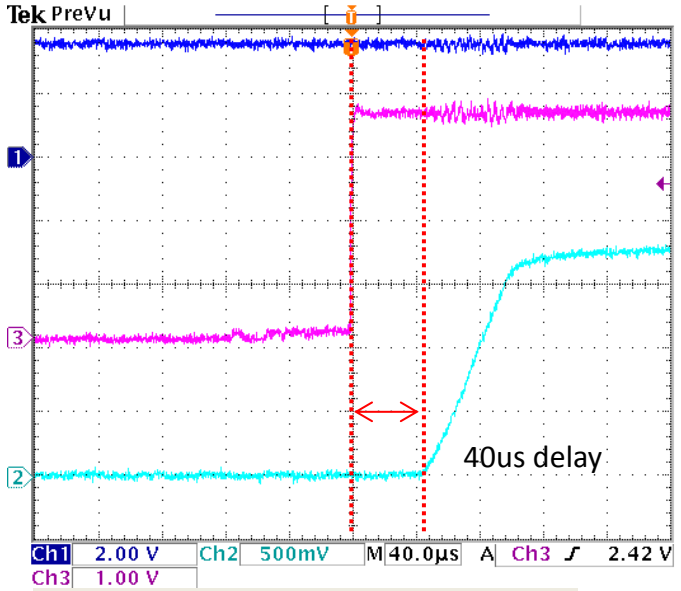


EVM waveform



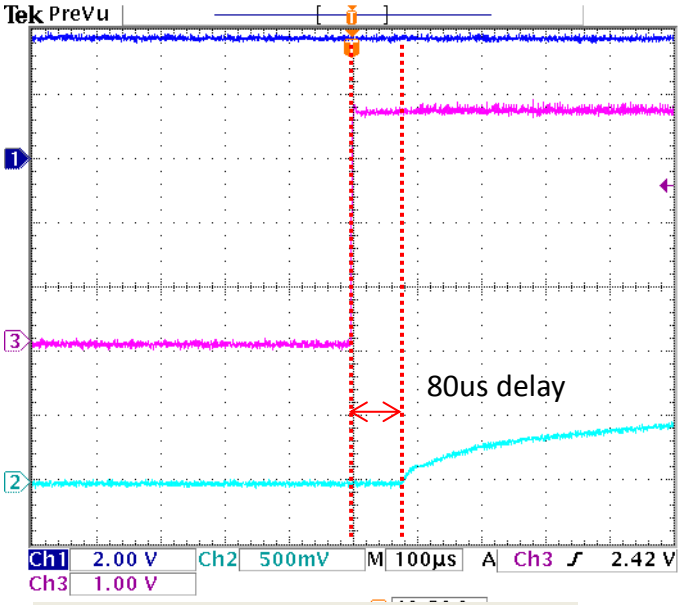
CH1:VIN
CH2:VOUT
CH3:EN

SS Cap=0.01uF waveform(400us/div)



CH1:VIN
CH2:VOUT
CH3:EN

SS Cap=2.2nF waveform



CH1:VIN
CH2:VOUT
CH3:EN

SS Cap=0.01uF waveform(100us/div)

When changing the capacitance of the SS capacitor,
A difference occurs in the delay time until the output voltage starts.
1. Please tell me the reason why the delay time is different.
2.Please tell me the relational expression between the SS capacitor and the delay time.