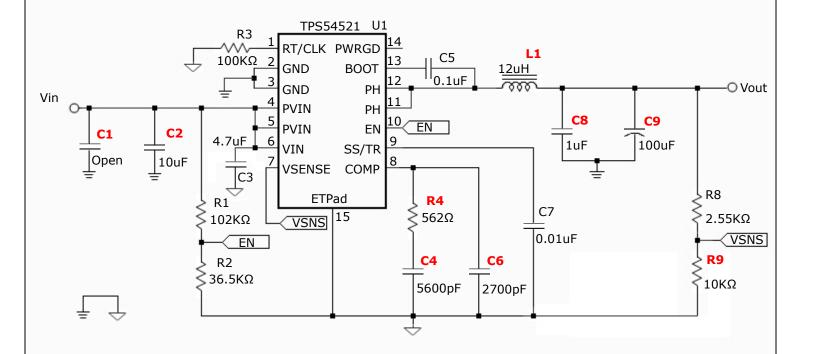
SwitcherPro Design Report Schematic

Design Name: TPS54521` **Part:** TPS54521

VinMin: 11V VinMax: 12V Vout: 1V Iout: 0.27A



(i) Please refer to the datasheet section 'Enable and Adjusting Under-Voltage Lockout' for details on UVLO resistor calculations.

SwitcherPro Design Report Analysis - Main

Design Name: TPS54521` **Part:** TPS54521

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	11.00	-	12.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	240	-	-	5.9
UVLO(Start) Volts - V	-	-	-	-	-	-	-	4.47	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	3.98	-
Switching Frequency KHz - KHz	-	-	-	-	495	-	-	-	-
Slow Start ms - ms	-	-	-	-	3.48	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	440	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	12

SwitcherPro Design Report Analysis - Output1

Design Name: TPS54521` **Part:** TPS54521

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	1.000	-	-	-	-	0.970	-	1.038
Output Ripple mVp-p - mVp-p	-	-	-	-	-	20	-	-	29.7
Output Current Amps - A	-	-	0.267	0.001	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.196	-	0.198
Current Limit Threshold Amps - A	-	-	-	-	1.400	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-12	-
Phase Margin Deg Deg.	-	-	-	60	-	-	-	87	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	81	-	81
Lower FET RDSon mOhms - mΩ	-	-	-	-	-	-	66	-	66
Duty Cycle % - %	-	-	-	-	-	-	8.6	-	9.3
On Time Min (switch) ns - ns	-	-	-	-	-	-	144.2	-	236.0
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	43	-

SwitcherPro Design Report Stress Results

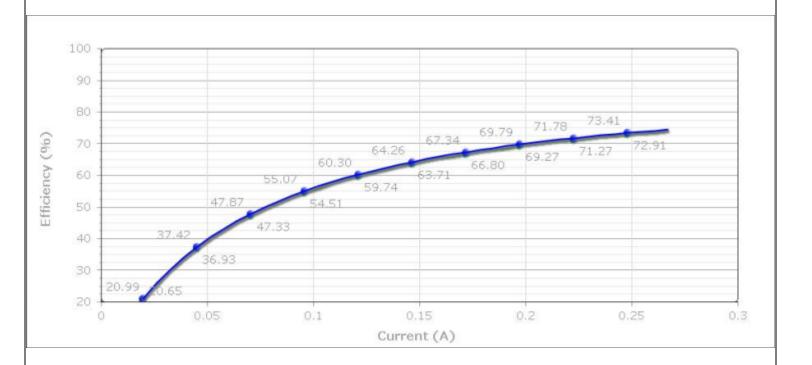
Design Name: TPS54521` **Part:** TPS54521

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C2 (High Freq. Input Cap)	25V	12.1V	3.5A	78mA	-	6uW	-
C9 (Bulk Output Cap)	35V	1V	0.67A	38mA	-	220uW	-
C8 (High Freq. Output Cap)	25V	1V	3.5A	19mA	-	704nW	-
L1 (Output Inductor)	-	-	1.3A	0.27A	-	3mW	-
U1 (Converter)	20V	12.1V	6.2A	0.27A	-	91mW	27°C

SwitcherPro Design Report Efficiency

Design Name: TPS54521` **Part:** TPS54521

VinMin: 11V VinMax: 12V Vout: 1V Iout: 0.27A

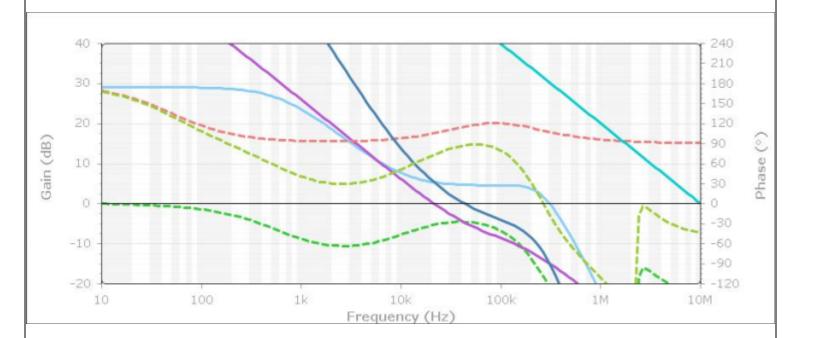


Efficiency For Vin Max

Efficiency For Vin Min

SwitcherPro Design Report Loop Response

Design Name: TPS54521` **Part:** TPS54521



- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

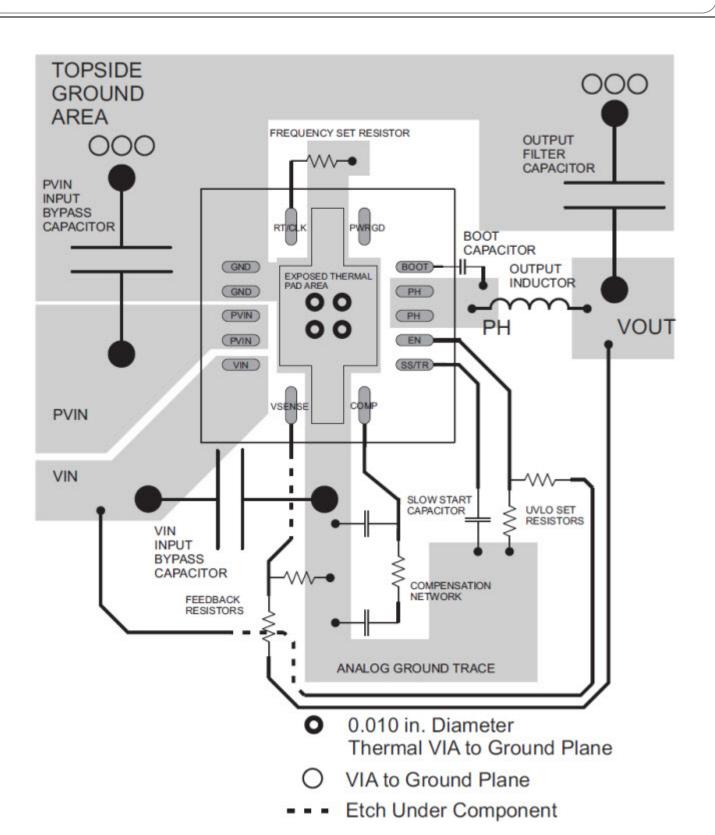
SwitcherPro Design Report Bill of Materials

Design Name: TPS54521` **Part:** TPS54521

Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C2	1	C3225X7R1E106M	Capacitor, Ceramic, 10uF, 25V, 20%	TDK	C3225 1210	8	1
С3	1	Standard	Capacitor, Ceramic, 4.7uF, 25V, 10%	Standard	0805	3	1
C4	1	Standard	Capacitor, Ceramic, 5600pF, 16V, 10%	Standard	0603	2	1
C5	1	Standard	Capacitor, Ceramic, 0.1uF, 16V, 20%	Standard	0603	2	1
C6	1	Standard	Capacitor, Ceramic, 2700pF, 16V, 10%	Standard	0603	2	1
C7	1	Standard	Capacitor, Ceramic, 0.01uF, 16V, 20%	Standard	0603	2	1
C8	1	C1608X5R1A105K	Capacitor, Ceramic, 1uF, 25V, 10%	TDK	0603	0	0
С9	1	EEEFC1V101P	Capacitor, Electrolytic, 100uF, 35V, 20%	Panasonic	Radial Can	86	12
L1	1	PCH-27-123	Inductor, 12uH, 1.3A, 37mΩ	CoilCraft	Unshielded	104	7
R1	1	Standard	Resistor, SurfaceMount, 102KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 36.5KΩ, 100mW, 1%	Standard	0603	2	1
R3	1	Standard	Resistor, SurfaceMount, 100KΩ, 100mW, 1%	Standard	0603	2	1
R4	1	Standard	Resistor, SurfaceMount, 562Ω, 100mW, 1%	Standard	0603	2	1
R8	1	Standard	Resistor, SurfaceMount, 2.55KΩ, 100mW, 1%	Standard	0603	2	1
R9	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54521	IC, Converter, 14 pins	Texas Instruments, Inc.	QFN-Power PAD	13	1

SwitcherPro Design Report Layout

Design Name: TPS54521` **Part:** TPS54521



SwitcherPro Design Report Layout Notes

Design Name: TPS54521` **Part:** TPS54521

VinMin: 11V VinMax: 12V Vout: 1V Iout: 0.27A

TPS54521

Layout is a critical portion of good power supply design. The top layer should contain the main power traces for VIN, VOUT, and the PH node. The top layer should also have connections for the remaining pins of the TPS54521 and a large top side area filled with ground. The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS54521 device to provide a thermal path from the exposed thermal pad land to ground. The GND pin should be tied directly to the exposed thermal pad under the IC. For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.

There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the PVIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the PVIN pins, and the ground connections. The VIN pin must also be bypassed to ground using a low ESR ceramic capacitor with X5R or X7R dielectric. Make sure to connect this capacitor to the quiet analog ground trace rather than the power ground trace of the PVIN bypass capacitor.

Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The output filter capacitor ground should use the same power ground trace as the PVIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width. The small signal components should be grounded to the analog ground path as shown.

The RT/CLK pin is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.