

12V\_VDD\_A EN/UVLO Voltage rising threshold typ 1.05V

+12V DC Input

[SILK : VCCINT\_0.85]

0.85V, 17A Typical

EN\_FPGA\_1ST

Fsw = 550kHz  
OCP = 30A/39A

It must be Kelvin Connection

ZYNQ\_3.3V

=>FPGA