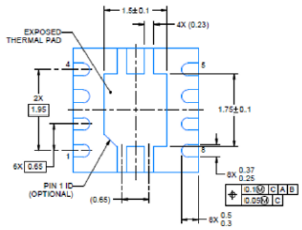
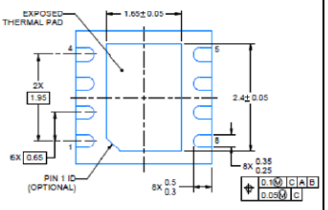
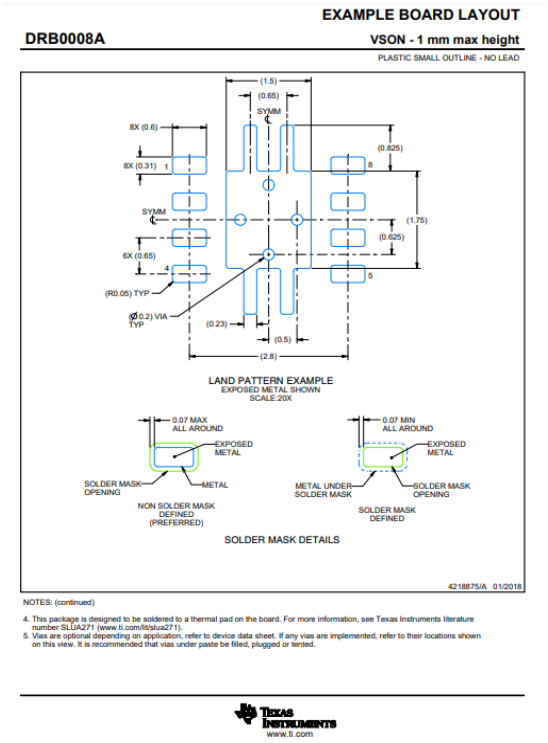
TPS61042DRB New package qualified

One of my customers knows that a new package made at TI CDAT assembly site were qualified as an additional package of TPS61042DRB via PCN# 20230719001.1

Package outline drawing:

	TI Malaysia	TI CDAT
		
Exposed Pad Size	1.50 x 1.75 mm	1.65 x 2.40 mm

They designed TPS61042DRB foot pattern on their PCB by copying example board layout on page 27 of the device datasheet.
Their stencil design is same. It was designed by copying example stencil design on page 28 of the datasheet.



EXAMPLE BOARD LAYOUT

DRB0008A — VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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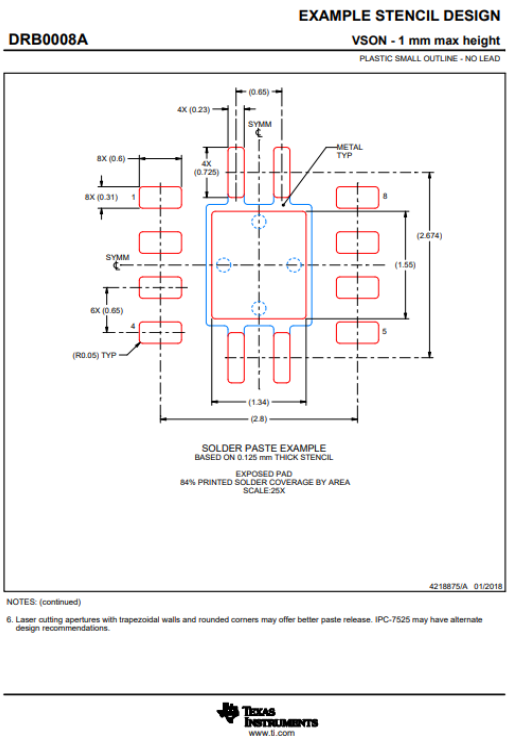

EXAMPLE STENCIL DESIGN

DRB0008A — VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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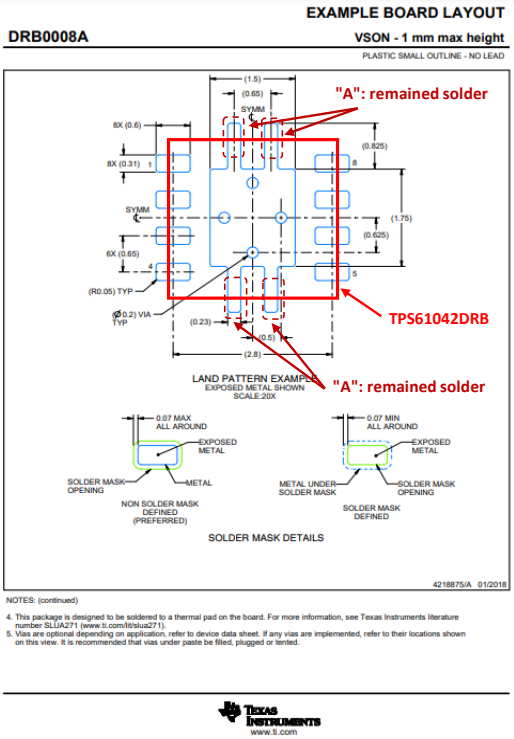
They think that remained solder of pattern "A" would become solder ball when the package made at TI CDAT is soldered without PCB footpattern changing and they worry that this solder ball would cause any trouble.



[Question]

What do TI think about this? They want to hear TI thought.

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