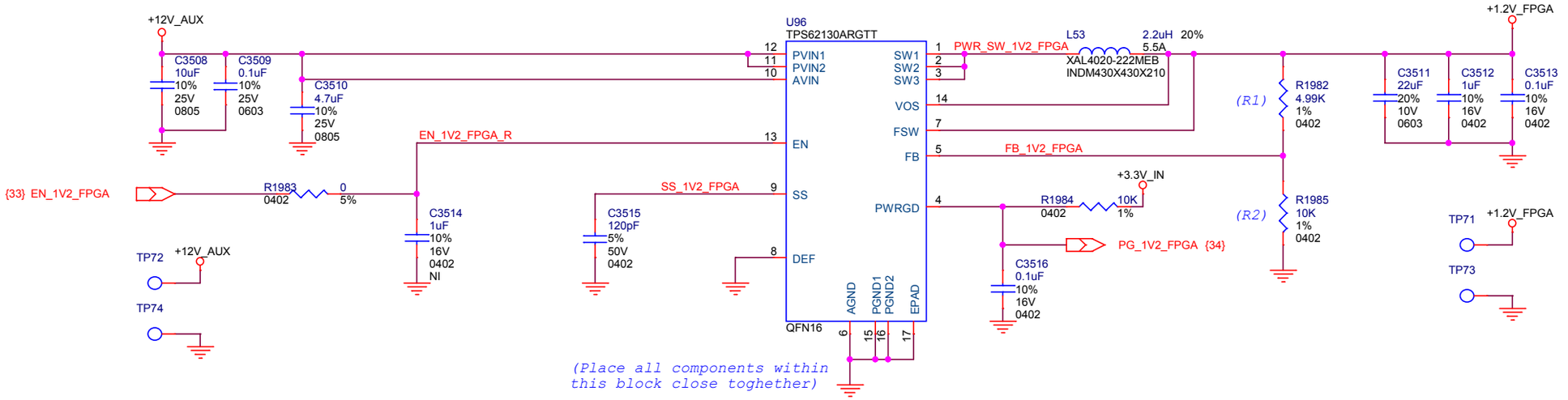
+1.2V_FPGA @ 3A Max

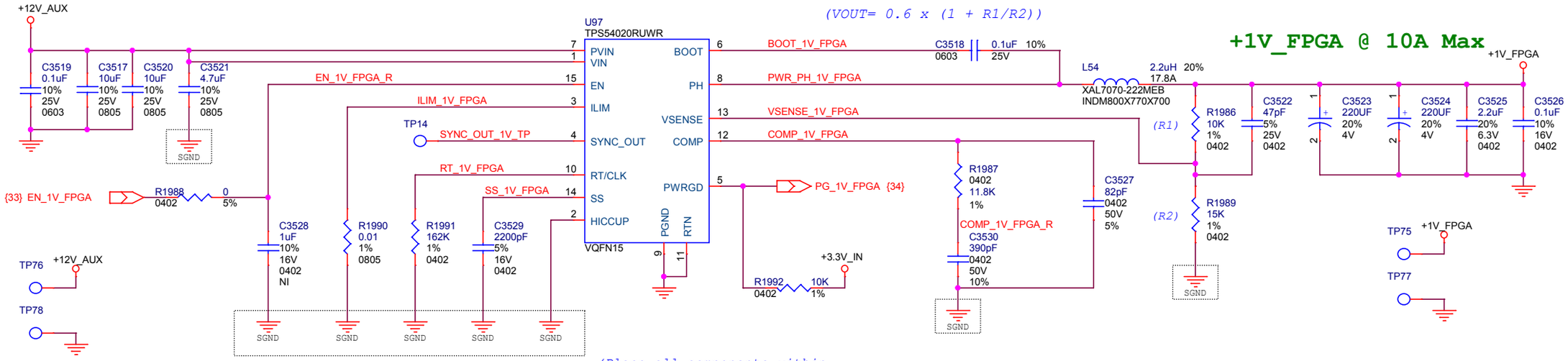
(VOUT = 0.8 x (1 + R1/R2))



(Place all components within this block close toghether)

+1V_FPGA @ 10A Max

(VOUT= 0.6 x (1 + R1/R2))



(Place all components within this block close toghether)

(Please refer layout guideline in Datasheet's TPS54020)

VERIK SYSTEMS

Title: +1V_FPGA, +1.2V_FPGA				
Size: B	Document Number: V-xxxxx-xxxxx	Engineer: VEriK	Drawn By: VEriK	Rev: 0.6
Date: Monday, June 29, 2015	Sheet 29 of 118			