TPS62240 Simulation Question

This reason for this analysis is to characterize the entire PDN (power distribution network), i.e., it’s output/source impedance vs frequency, which allows me to design for a specific target voltage ripple.

The lower frequency load current from DC to ~10kHz should be serviced by the voltage regulator. From ~10kHz to ~100MHz, the current is serviced by decoupling capacitors. Beyond ~100MHz, the current is serviced by PCB plane capacitance. The analytical approach to decoupling requires understand all 3 pieces. I am asking you about the first, the regulator.

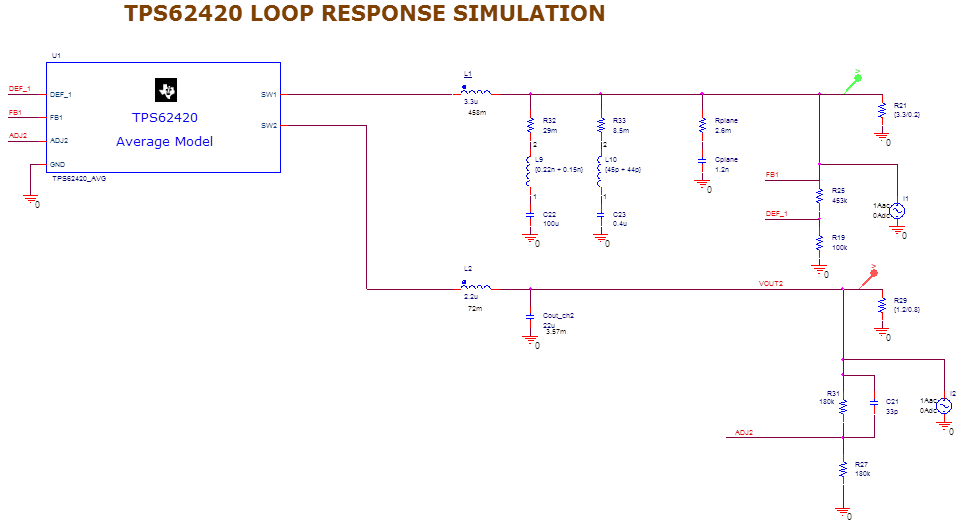
The Cadence Pspice project that comes with the average models (for some of your converters) is setup to analyze open-loop gain. All I’m doing is moving the AC stimulus (not possible on all the models—some are embedded in the model) from inside the loop, to outside the loop, which means it’s now a closed loop simulation. Then, I just inject an AC current into the output and at the same time observe the voltage. Then I just plot Z = V/I. This is effectively the closed-loop output impedance. Another way of doing this would be to divide the open-loop output impedance by the loop gain. Since I don’t know the open-loop output impedance from the datasheet, I have to derive it. There are papers on how to derive the open-loop output impedance and I could use the loop-gain curve from the datasheets but why do all that work?

To one of your earlier points, this is output impedance not resistance so a 10mohm target is not impossible to achieve. It’s based on loop gain, the inductor, the DC load (R) and output capacitance.

I switched to the TPS62420 because it appeared to have a lower output impedance, so I’ll be using that in all the examples below. Unfortunately, there weren’t many parts to choose from after filtering on parts that had an average spice model that also fit my design requirements and efficiency. If this is accurate, you all should add some more models!

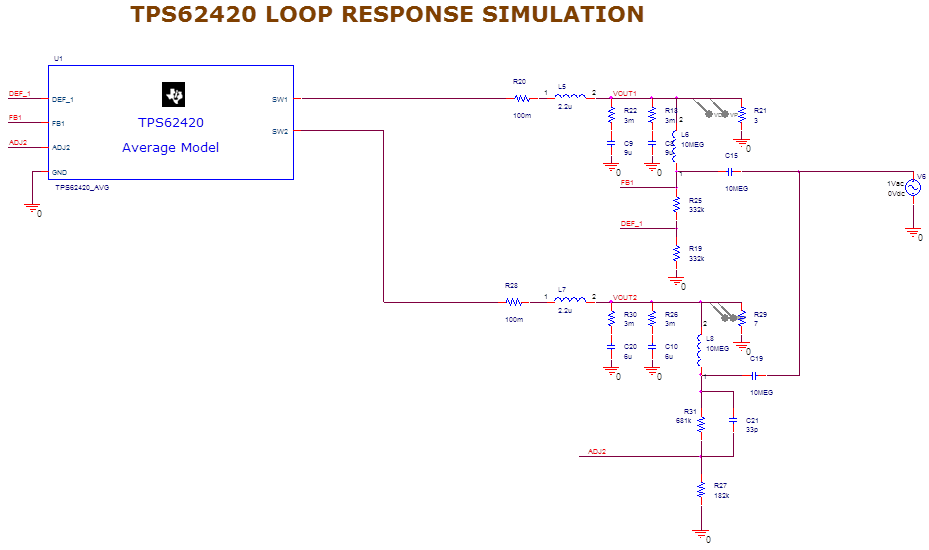
Here is a link to the Pspice average model: <http://www.ti.com/lit/zip/slim129>

 Here’s the default model:

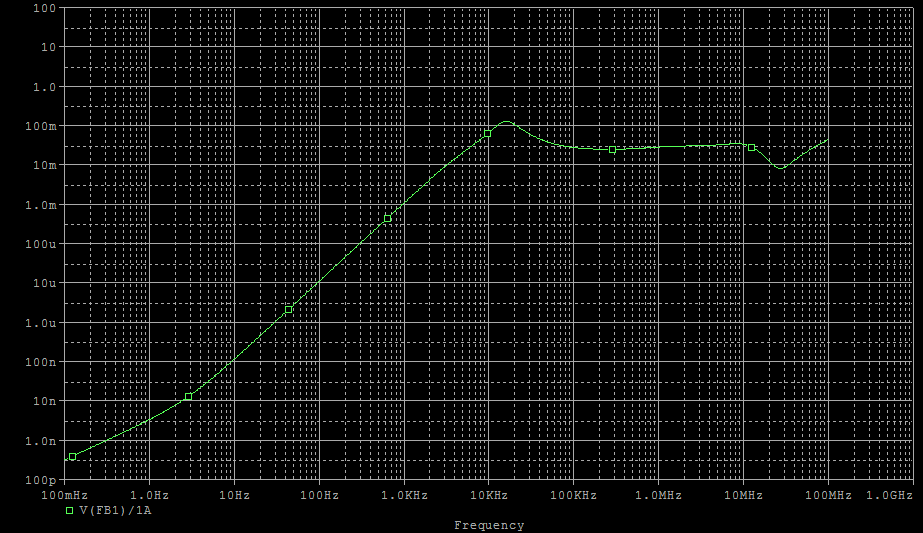


There is an AC voltage injected into the loop to simulate the open-loop conditions.

Now here is my modification to measure output impedance (with my own caps/inductor values):



Here is the plot measuring the output impedance:



My target is 33mohm from DC to 100MHz, but you can see that the regulator quickly reaches that at 10kHz. That is almost impossible to compensate for with capacitors. Fortunately, it’s probably OK because I don’t have any demand at that frequency (that I know of yet).

I’m injecting a ripple current to measure the voltage reaction to that dynamic load current. This gives me an impedance curve (Z = VOUT/IAC). Now, I can multiply my load’s current PSD times this curve, it will give me the ripple voltage.