

TPS54335A Board Layout

TPS62480 Board Layout

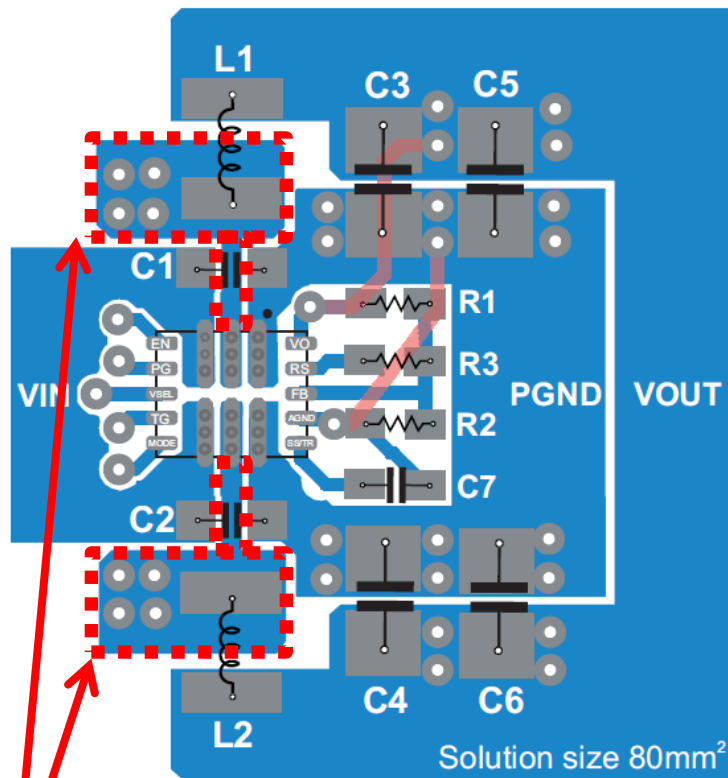
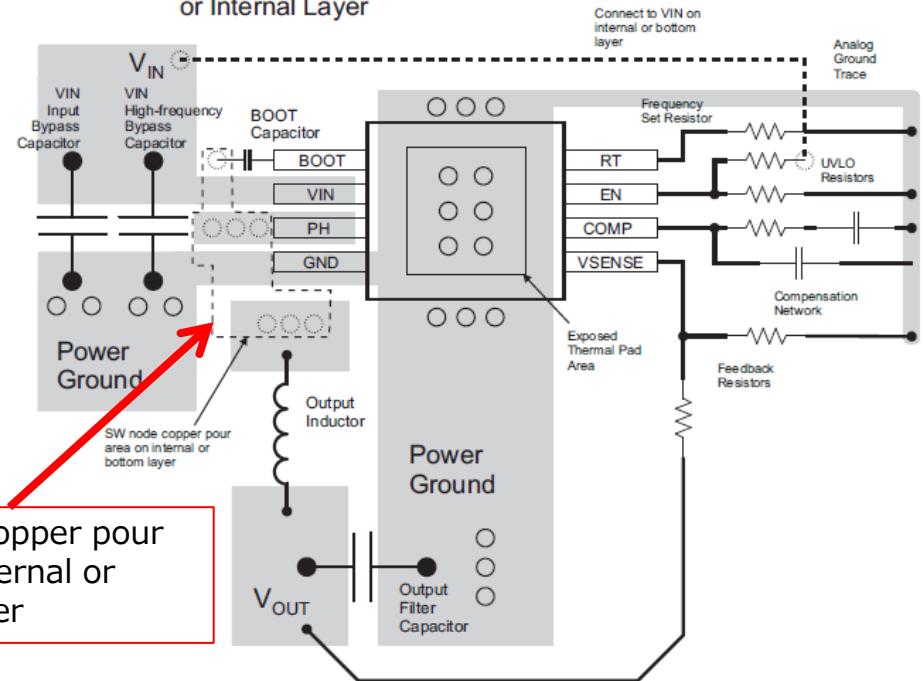


Figure 46. TPS62480 Board Layout

Can SW node copper pour area on internal or bottom layer?

10.2 Layout Example

- Via to Power Ground Plane
- Via to SW Copper Pour on Bottom or Internal Layer



Note: Pin 8 for the TPS54336A device is SS. Connect an SS capacitor instead of an RT resistor from pin 8 to GND.

Figure 55. TPS54335A Board Layout

There is SW node copper pour area on internal or bottom layer of TPS54335A.
Can TPS62480 use SW node in the same way as TPS54335A?