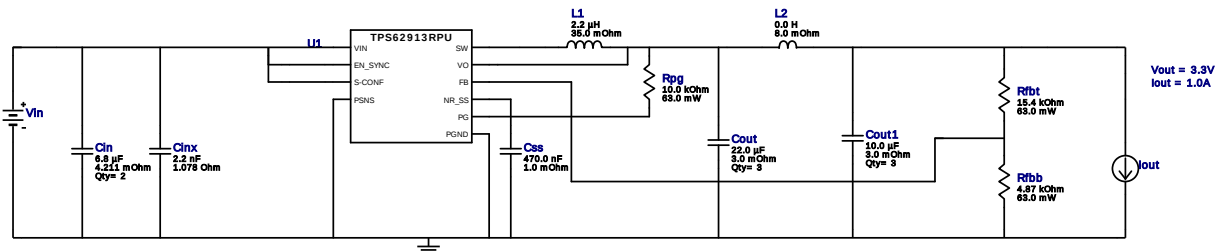


VinMin = 12.0V
VinMax = 12.0V
Vout = 3.3V
Iout = 1.0A

Device = TPS62913RPUR
Topology = Buck
Created = 2021-10-29 03:52:55.362
BOM Cost = \$2.60
BOM Count = 16
Total Pd = 0.21W

WEBENCH® Design Report

Design : 742 TPS62913RPUR
TPS62913RPUR 12V-12V to 3.30V @ 1A



Design Alerts

TPS62913 Design

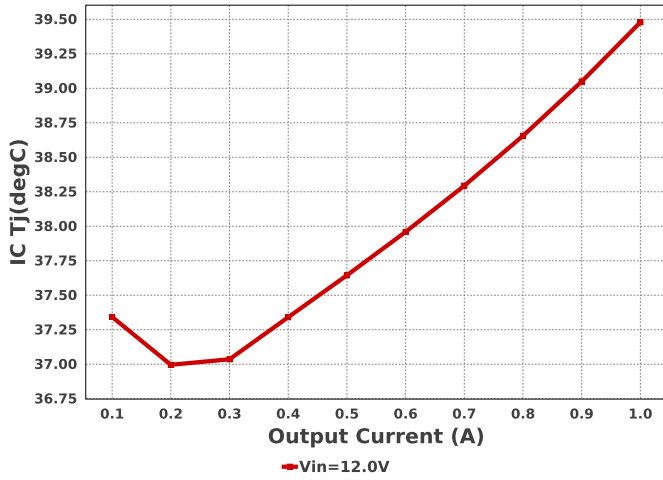
The TPS62913 supports a second LC ferrite bead output filter to achieve lowest output voltage ripple. To enable this filter in the design, use the Second Stage Output Filter dropdown option from Advanced options on the left side. Please refer to the TPS62913 datasheet for more information.

Electrical BOM

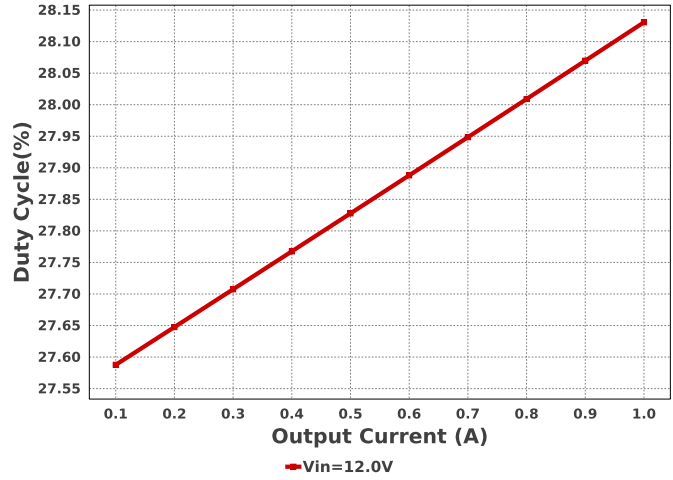
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cin	TDK	C1608X5R1E685K080AC Series= X5R	Cap= 6.8 uF ESR= 4.211 mOhm VDC= 25.0 V IRMS= 2.5341 A	2	\$0.17	0603 5 mm ²
Cinx	TDK	CGA2B2X7R1H222K050BA Series= X7R	Cap= 2.2 nF ESR= 1.0779 Ohm VDC= 50.0 V IRMS= 264.071 mA	1	\$0.01	0402 3 mm ²
Cout	MuRata	GRM21BR61A226ME44L Series= X5R	Cap= 22.0 uF ESR= 3.0 mOhm VDC= 10.0 V IRMS= 3.84 A	3	\$0.13	0805 7 mm ²
Cout1	Kemet	C0805C106K8PACTU Series= X5R	Cap= 10.0 uF ESR= 3.0 mOhm VDC= 10.0 V IRMS= 11.43 A	3	\$0.03	0805 7 mm ²
Css	MuRata	GRM188R60J474KA01D Series= X5R	Cap= 470.0 nF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 0.0 A	1	\$0.02	0603 5 mm ²
L1	Abrakon Corporation	ASPI-0530HI-2R2M-T2	L= 2.2 uH 35.0 mOhm	1	\$0.41	ASPI-0530HI 55 mm ²
L2	Würth Elektronik	782853200	L= 0.0 H 8.0 mOhm	1	\$0.09	0805 7 mm ²
Rfbb	Vishay-Dale	CRCW04024K87FKED Series= CRCW..e3	Res= 4.87 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rfbb	Vishay-Dale	CRCW040215K4FKED Series= CRCW..e3	Res= 15.4 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
Rpg	Vishay-Dale	CRCW040210K0FKED Series= CRCW..e3	Res= 10.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
U1	Texas Instruments	TPS62913RPUR	Switcher	1	\$1.22	RPU0010A-MFG 9 mm ²

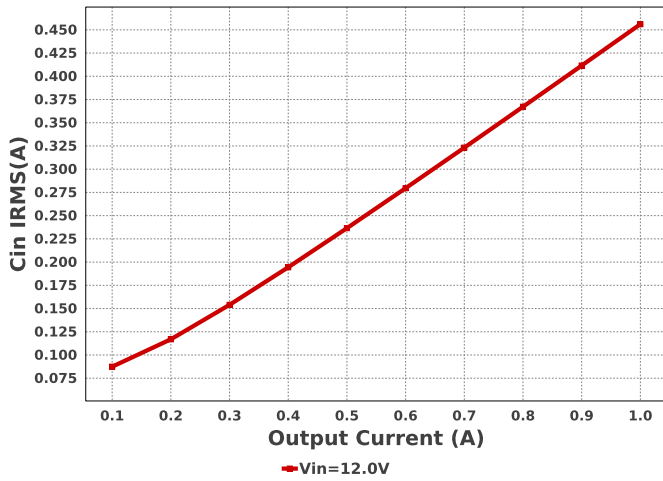
IC Tj



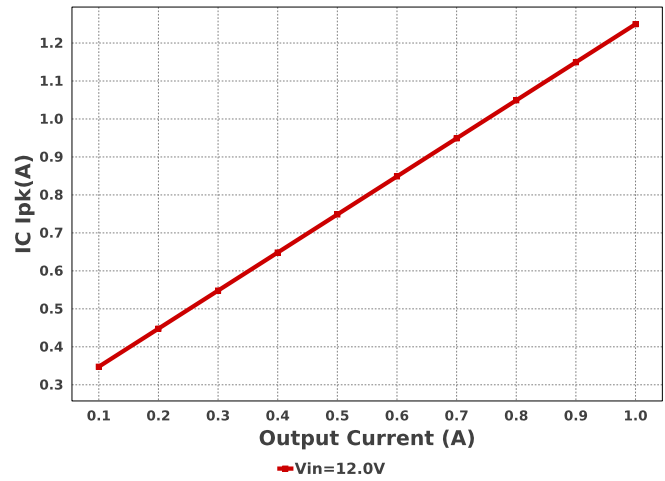
Duty Cycle



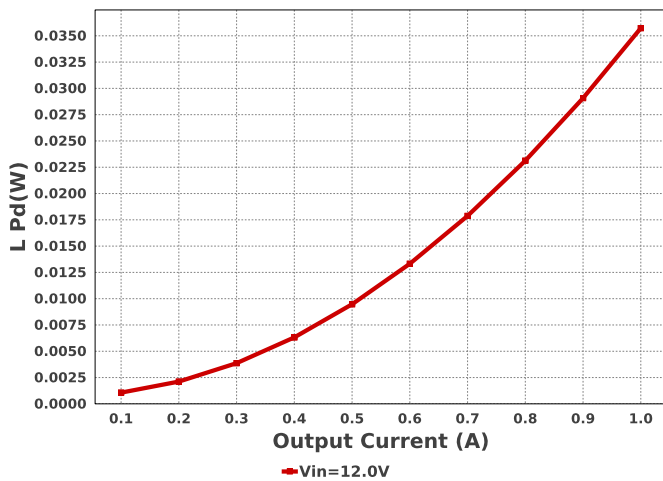
Cin IRMS



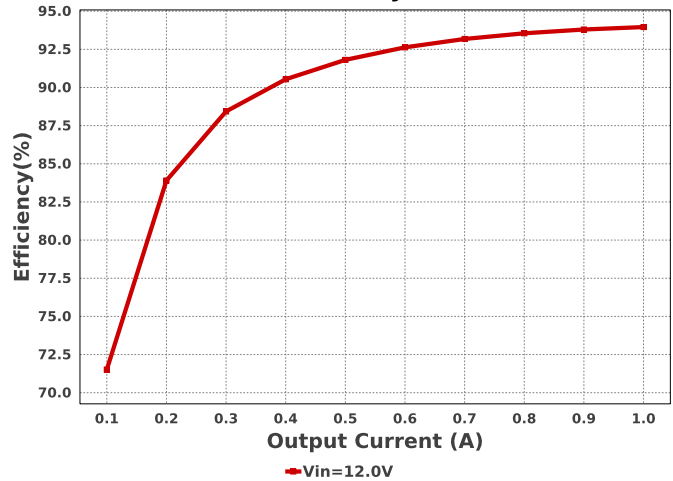
IC Ipk

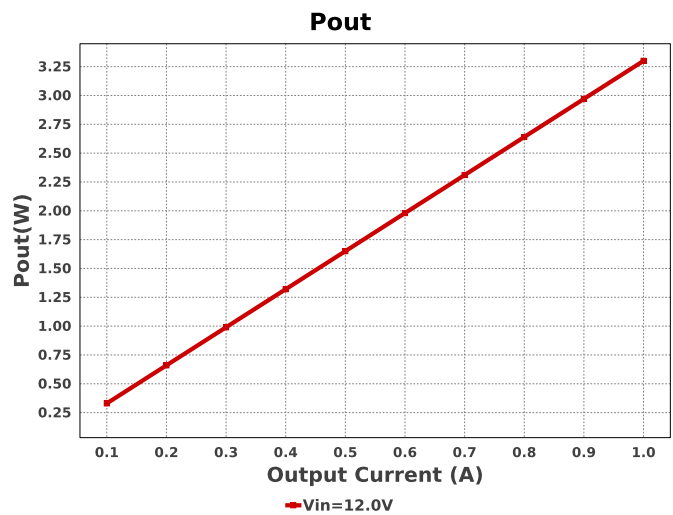
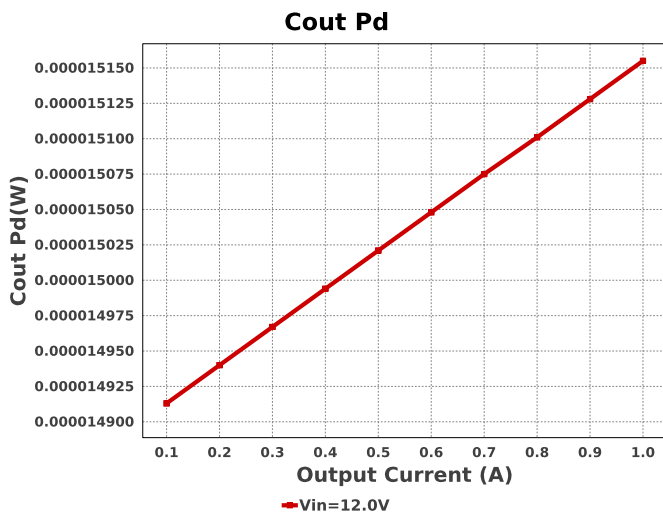
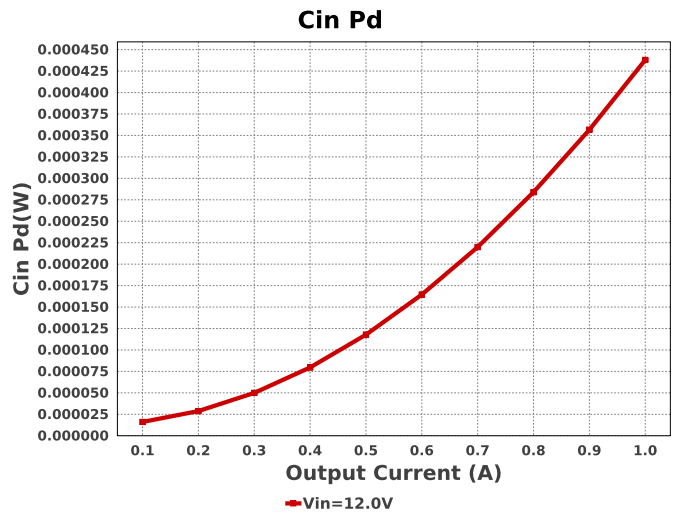
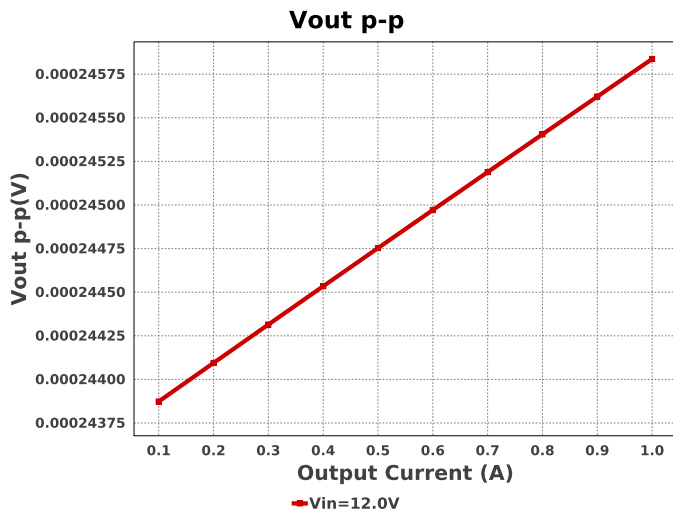
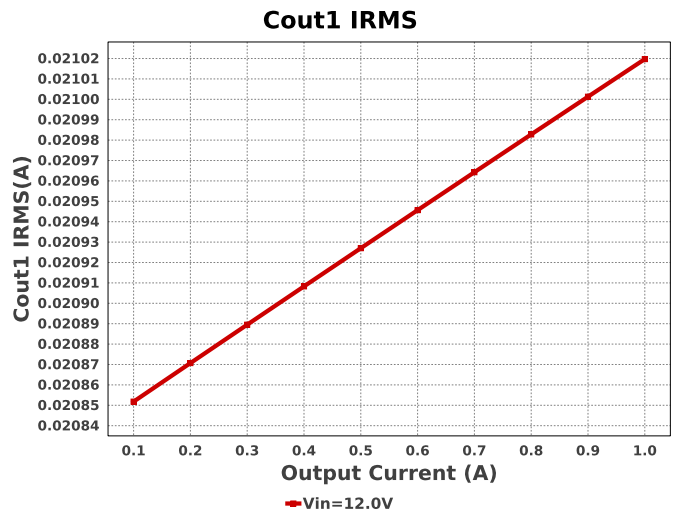
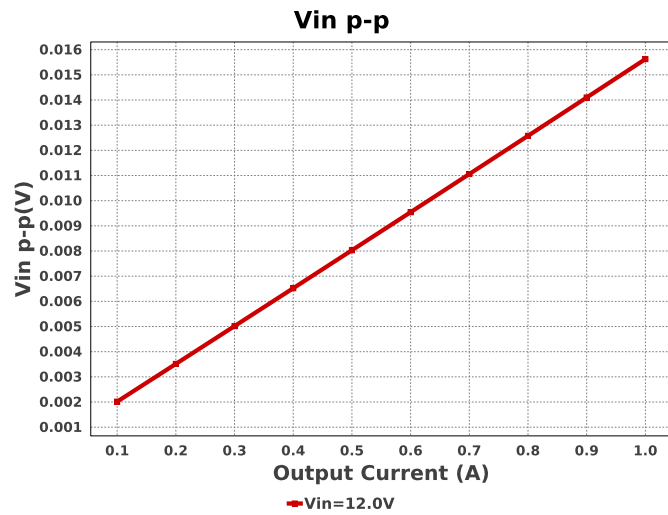


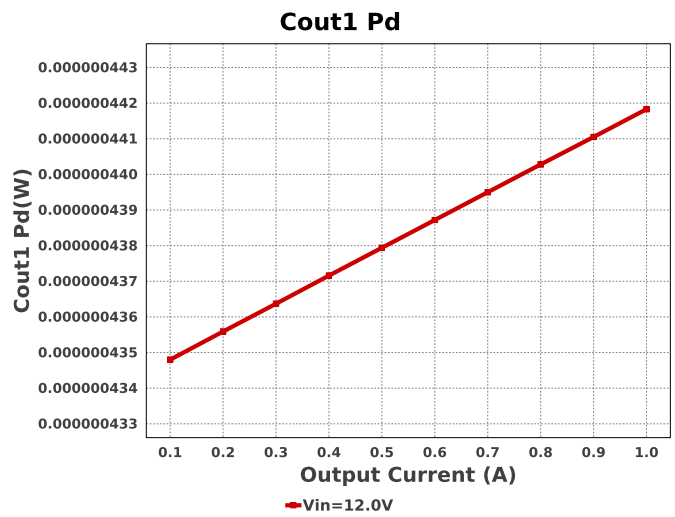
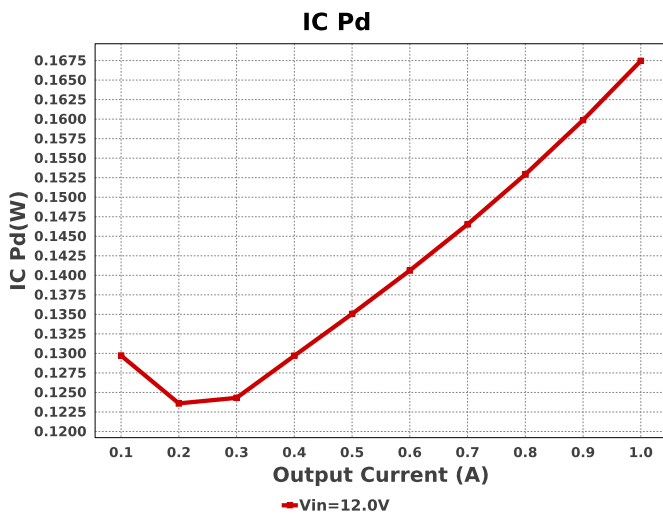
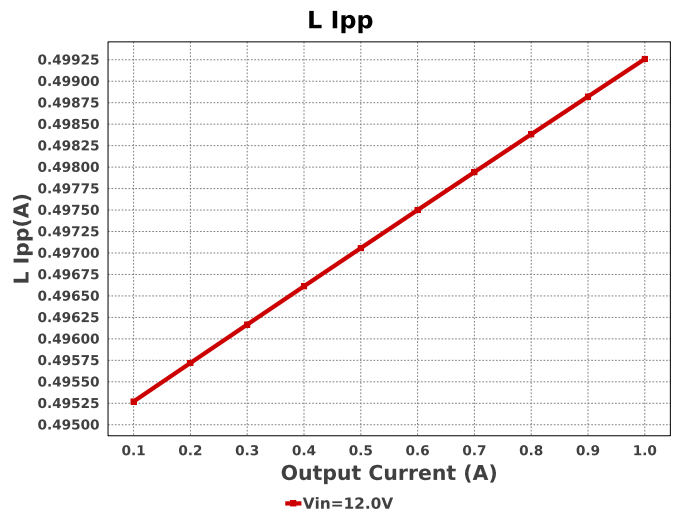
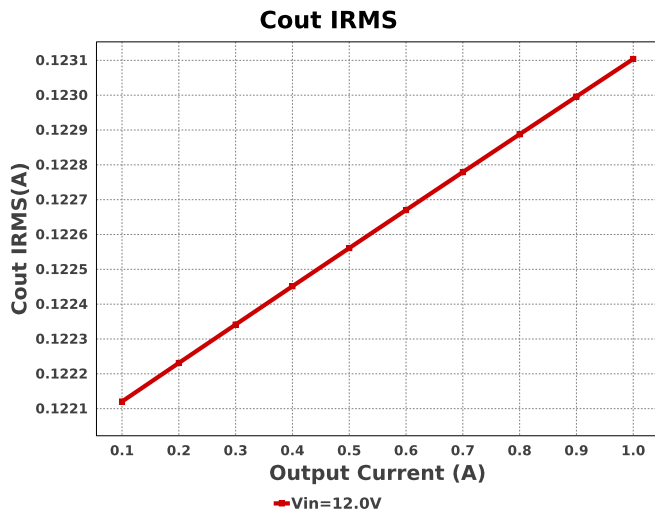
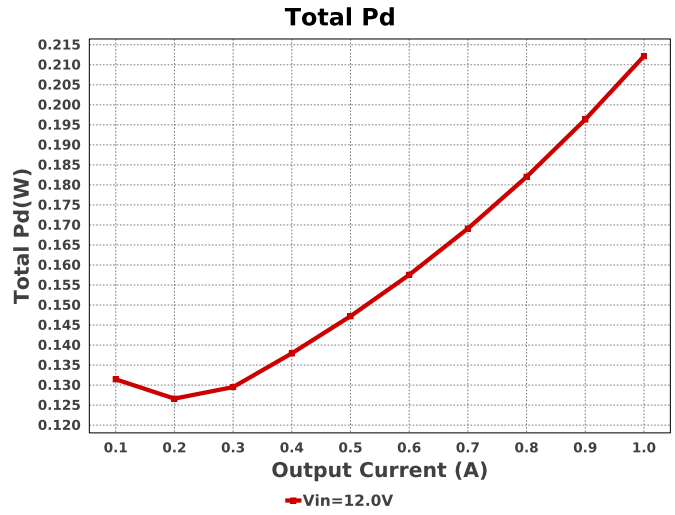
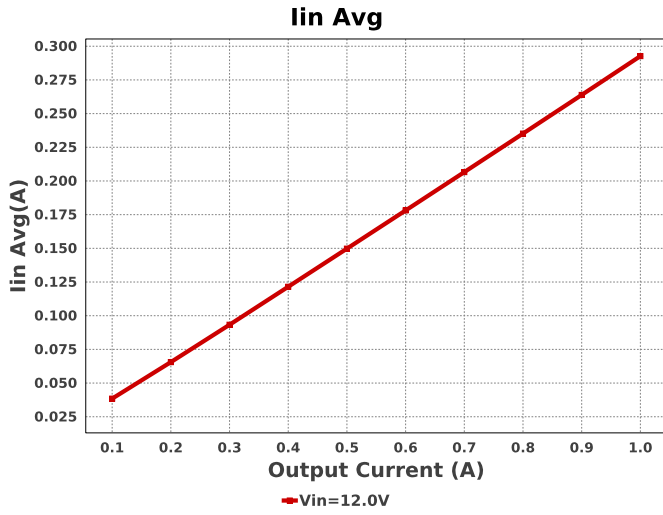
L Pd

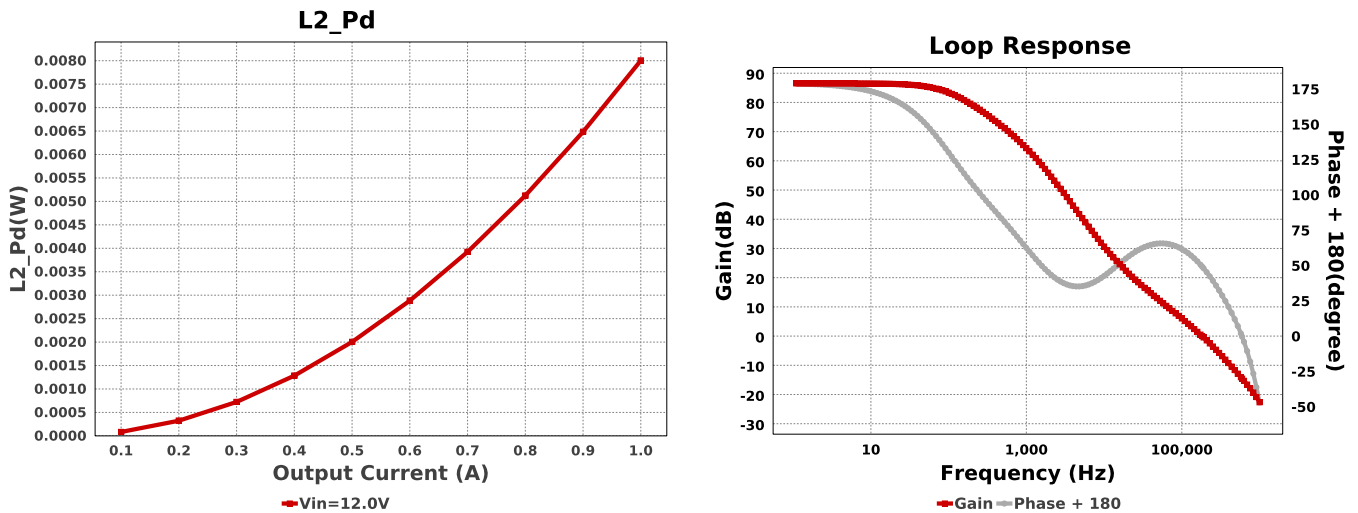


Efficiency









Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	456.088 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	437.98 μ W	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	123.104 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	15.155 μ W	Capacitor	Output capacitor power dissipation
5.	Cout1 IRMS	21.02 mA	Capacitor	Output capacitor1 RMS ripple current
6.	Cout1 Pd	441.83 nW	Capacitor	Output capacitor1 power dissipation
7.	IC Ipk	1.25 A	IC	Peak switch current in IC
8.	IC Pd	167.46 mW	IC	IC power dissipation
9.	IC Tj	39.478 degC	IC	IC junction temperature
10.	ICThetaJA	56.6 degC/W	IC	IC junction-to-ambient thermal resistance
11.	Iin Avg	292.68 mA	IC	Average input current
12.	Ipp percentage	49.926 %	Inductor	Inductor ripple current percentage (with respect to average inductor current)
13.	L Ipp	499.26 mA	Inductor	Peak-to-peak inductor ripple current
14.	L Pd	35.727 mW	Inductor	Inductor power dissipation
15.	L2_Pd	8.004 mW	Inductor	Inductor2 power loss
16.	Cin Pd	437.98 μ W	Power	Input capacitor power dissipation
17.	Cout Pd	15.155 μ W	Power	Output capacitor power dissipation
18.	Cout1 Pd	441.83 nW	Power	Output capacitor1 power dissipation
19.	IC Pd	167.46 mW	Power	IC power dissipation
20.	L Pd	35.727 mW	Power	Inductor power dissipation
21.	L2_Pd	8.004 mW	Power	Inductor2 power loss
22.	Total Pd	212.17 mW	Power	Total Power Dissipation
23.	BOM Count	16	System	Total Design BOM count
24.	Cross Freq	182.427 kHz	Information	Bode plot crossover frequency
25.	Duty Cycle	28.131 %	System	Duty cycle
26.	Efficiency	93.959 %	Information	Steady state efficiency
27.	FootPrint	137.0 mm ²	System	Total Foot Print Area of BOM components
28.	Frequency	2.2 MHz	Information	Switching frequency
29.	Gain Marg	-14.558 dB	System	Bode Plot Gain Margin
30.	Iout	1.0 A	Information	Iout operating point
31.	Low Freq Gain	86.5 dB	System	Gain at 1Hz
32.	Mode	FCCM	Information	Conduction Mode
33.	Phase Marg	49.615 deg	System	Bode Plot Phase Margin
34.	Pout	3.3 W	Information	Total output power
35.	Total BOM	\$2.6	System	Total BOM Cost
36.	Vin	12.0 V	Information	Vin operating point

#	Name	Value	Category	Description
37.	Vin p-p	15.626 mV	System Information	Peak-to-peak input voltage
38.	Vout	3.3 V	System Information	Operational Output Voltage
39.	Vout Actual	3.33 V	System Information	Vout Actual calculated based on selected voltage divider resistors
40.	Vout Tolerance	2.042 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors at 25 degC
41.	Vout p-p	245.837 μ V	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	1.0	Maximum Output Current
SoftStart	5.0 ms	Soft Start Time (ms)
VinMax	12.0	Maximum input voltage
VinMin	12.0	Minimum input voltage
Vout	3.3	Output Voltage
base_pn	TPS62913	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of C_{in} and C_{out} , and the inductance and DC resistance of $L1$ before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

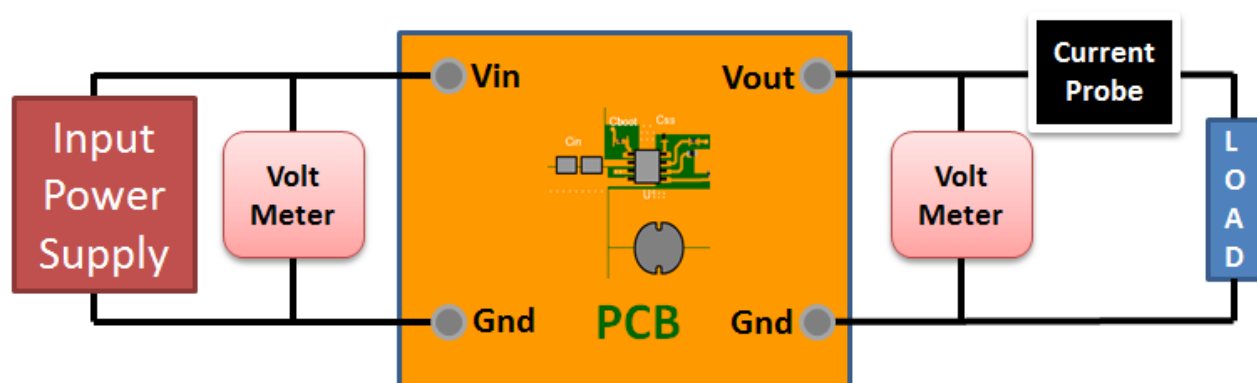
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab down to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 12.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to V_{in} and GND. Connect a digital volt meter and a load if needed to set the minimum load of the design from V_{out} and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between V_{in} and GND, a load is connected between V_{out} and GND and a current meter is connected in series between V_{out} and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : E2EC2B81AD3E5F56[v1]
2. **TPS62913** Product Folder : <http://www.ti.com/product/TPS62913> : contains the data sheet and other resources.

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