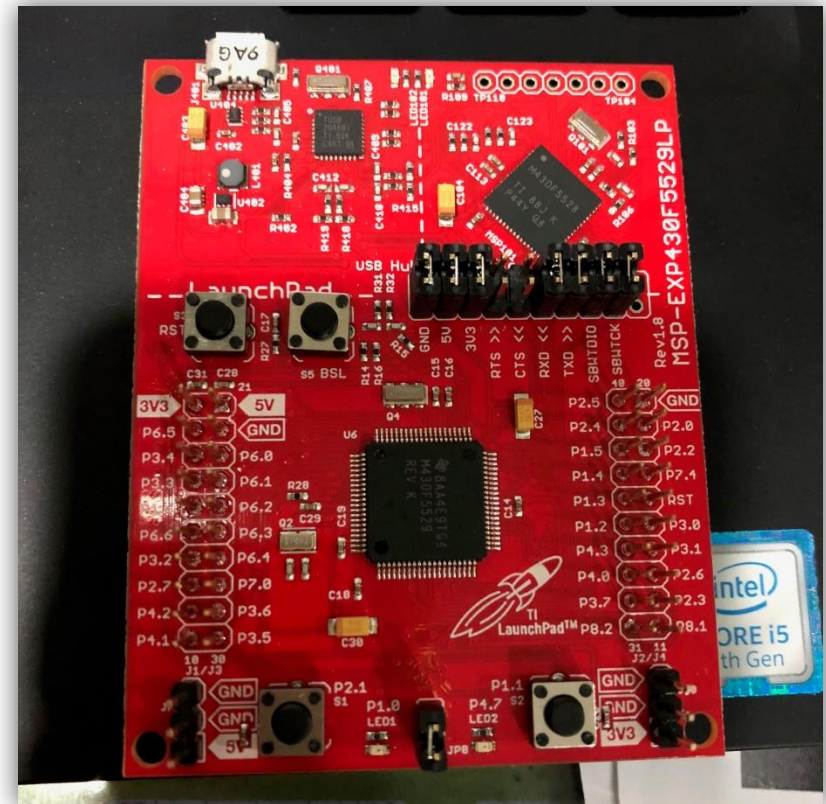
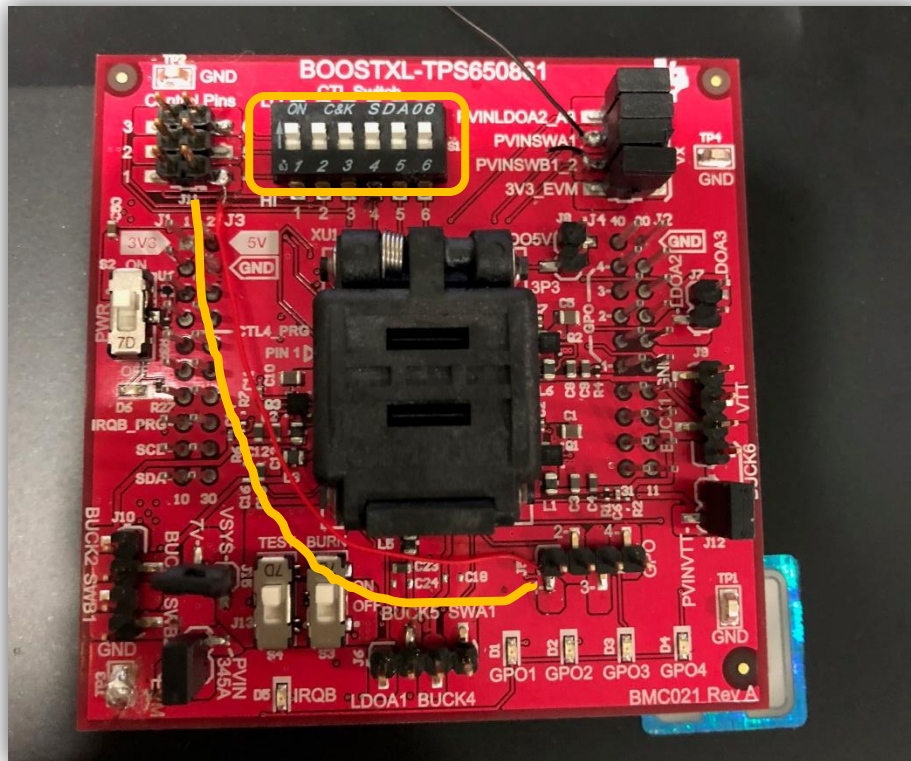


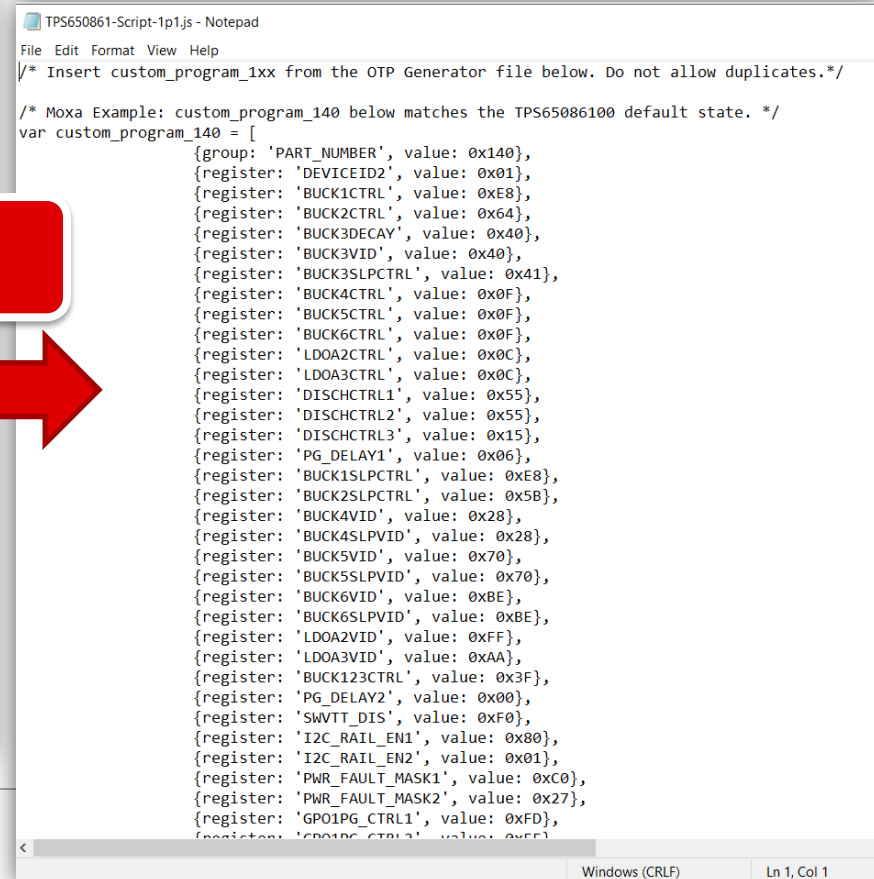
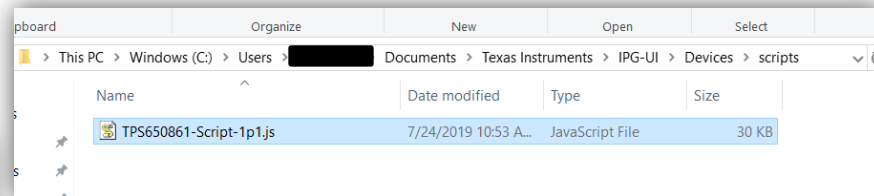
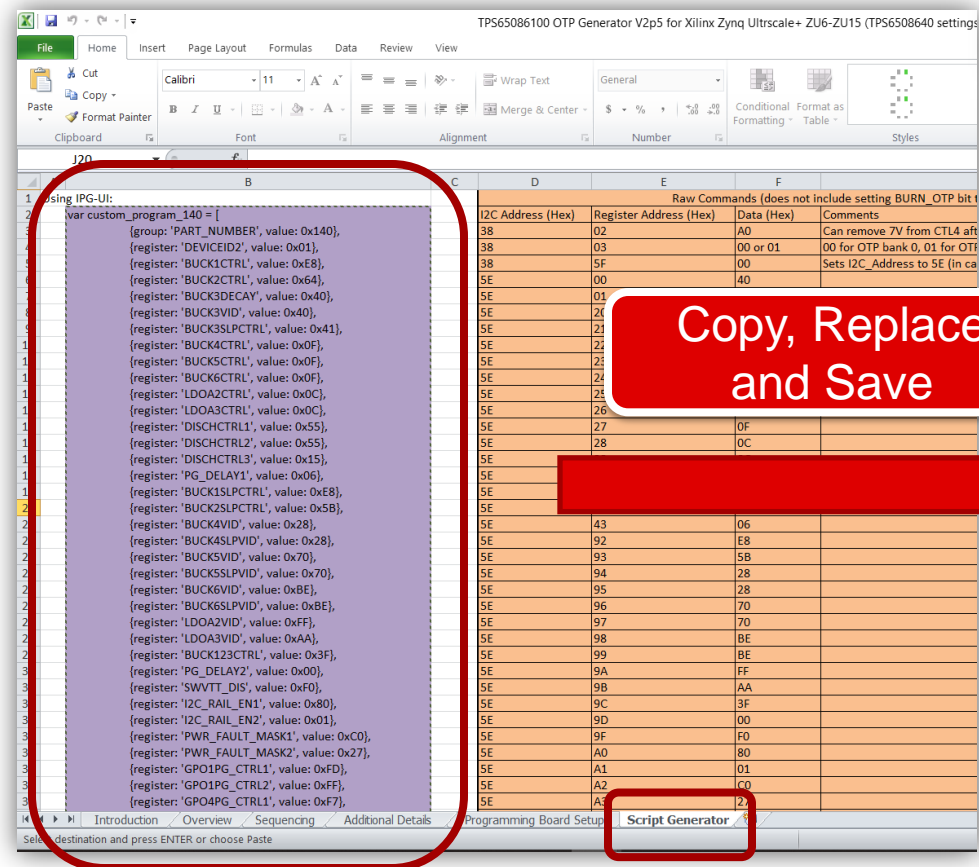
Hardware setup before programming

- Jumpers installed: J12, J13, all of J14, J15.
- Put S1 (CTL1-6) to on.
- CTL4 short to GPO1



Programming code procedure

- 1. Copy purple column in the "Script Generator" tab and paste and replace to TPS650861-Script-1p0.js file
- Note: Use TPS6508640 setting.



Programming code procedure

- 2. Open IPG-UI and make sure IPG-UI report hardware connected in the bottom.
- Read Register 0x05 and make sure the value is 04.

IPGUI - TPS650861

File GUI Settings Report About

New Project Open Project Save Project Save As Project

Introduction
Register Map
Single Register
Register Controls
Device Controls
Adapter Controls
Macros

I2C Address 0x5E Reg Address 05 Big Endian Addressing ☐
Reg Width 1 bytes

Register Name	Address	7	6	5	4	3	2	1	0	Value	W	R
SHUTDNSRC	0x05	0	0	0	0	0	1	0	0	04	W	R

SHUTDNSRC
This is the SHUTDNSRC register

COLDOFF R W
☐ PMIC shut down by CTL1
Not used. Asserted only in OTPs where CTL1 is used for emergency shutdown. Write a 1 to clear

UVLO R W
☒ PMIC shut down by UVLO
Asserted when PMIC was shut down due to UVLO event. Write a 1 to clear

PWR_FAULT R W
☐ PMIC shut down due to power fault
Asserted when PMIC was shut down due to power fault event. Write a 1 to clear

CRITTEMP R W
☐ PMIC shut down due to crit temp
Asserted when PMIC was shut down due to critical temperature. Write a 1 to clear

Adapter is not connected Hardware Not Connected TEXAS INSTRUMENTS

Programming code procedure

The screenshot displays the IPGUI - TPS650861 software interface. The top menu bar includes File, GUI Settings, Report, and About. Below the menu bar is a toolbar with New Project, Open Project, Save Project, and Save As Project. The left sidebar contains a navigation menu with Introduction, Register Map, Single Register, Register Controls, Device Controls, Adapter Controls, and Macros. The main content area is divided into two tabs: Programming and Power. The Programming tab is active, showing six numbered steps for the programming procedure:

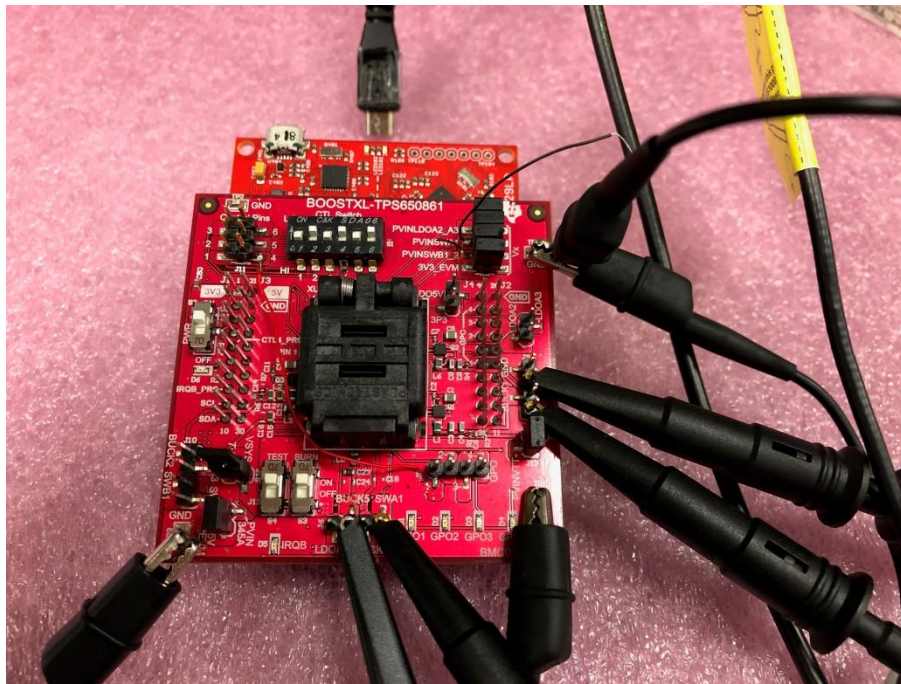
- (1) Test Mode**: Enables programming state. This button sets GPIO_12 of MSP430F5529 to output 3.3 V, resulting in 7V on PMIC CTL4 pin on BOOSTXL-TPS650861 board. After 400 ms, it sets the PROGRAMMING_STATE bit = 1b so 7V on CTL4 of PMIC can be removed. After 400 additional ms, it sets GPIO_12 of MSP430F5529 to output 0 V, returning CTL4 to normal. If not using BOOSTXL-TPS650861, 7V must be applied to CTL4 first or else the write will fail.
- (2) OTP Bank 0**: Selects the OTP bank to be programmed. This button writes to the OTP_BANK bits in the OTP_CTRL2 register. Only works in programming state.
- (3) 0x140**: Selects the OTP program to load into active (volatile) registers. The values chosen are the same as the values stored in the PART_NUMBER group in the DEVICEID1 register and the DEVICEID2 register.
- (4) Write**: Writes the selected OTP program into active (volatile) registers. This button does not program the OTP.
- (5) Check**: Checks each active (volatile) register to ensure that selected OTP program has properly loaded. Reports the first mismatched register or group if there is one. If the I2C address has been changed in the active (volatile) registers from the default (0x5E) then the I2C address dropdown
- (6) Program OTP**: Programs the selected OTP bank with the values in the active (volatile) registers. This button sets GPIO_2 of MSP430F5529 to output 3.3 V, resulting in 7 V on PMIC IRQB pin on BOOSTXL-TPS650861 board. After 400 ms, it sets the PROGRAM_OTP bit = 1b to start the internal OTP

Red arrows indicate the sequence of steps: (1) → (2) → (3) → (4) → (5) → (6). A large red arrow points from step (4) to step (5).

At the bottom, a status bar shows: Control: (3), Action: set_device_programming, Value: 320, Text Value 0x140. To the right, it says Hardware Not Connected and the Texas Instruments logo.

Tested Power performance

- Switch CTL5→CTL1→CTL3→CTL4 to HI in order and measure power performance.
- Note: Please ignore the position on CTL4 in this graph. We always put CTL4 to HI.



Measurement result

- The measurement result of power sequence is not align with TPS6508640 setting.

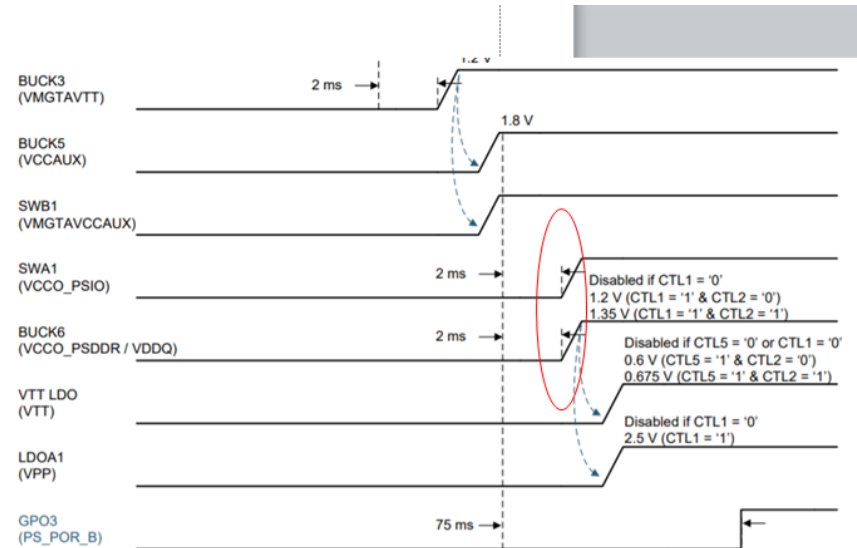
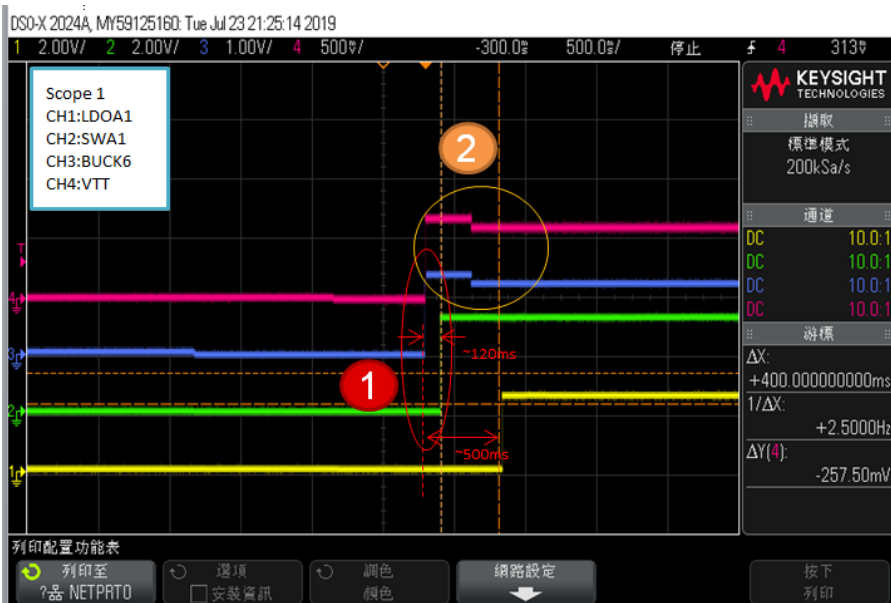


Figure 6-4. TPS6508640 Power-Up Sequence

Programming issue

- We doubt we did not program codes into TPS65086100. So we try to change buck5 voltage from 1.8V to 1V or 0.6V. And we use the programming procedure in previous slide. But buck5 voltage did not change and keep 1.8V. When I read register “BUCK5VID”, the register value keep the same (70).

Default Voltages			
Rail	Voltage (V)	Step Size:	Default VID
BUCK1_VID	3.300	25 mV	1110100
BUCK1_SLP_VID	-		1110100
BUCK2_VID	0.900	10 mV	0110010
BUCK2_SLP_VID	0.850		0101101
BUCK3_VID	1.200	25 mV	0100000
BUCK3_SLP_VID	-		0100000
BUCK4_VID	0.900	25 mV	0010100
BUCK4_SLP_VID	-		0010100
BUCK5_VID	1.000	25 mV	0011000
BUCK5_SLP_VID	-		0011000
BUCK6_VID	1.350	10 mV	1011111
BUCK6_SLP_VID	-		1011111
BUCK6 (CTL2 Alternate)	1.200		
LDOA1_VID	2.5		1010
LDOA2_VID	1.5		1111
LDOA2_SLP_VID	-		1111
LDOA3_VID	1.2		1010
LDOA3_SLP_VID	-		1010

★ BUCK5VID 0x96 0 1 1 1 0 0 0 0 70 W R ☐

Programming issue

- After we try to many setting, we write TPS6508640 code again. But we got different power performance.

