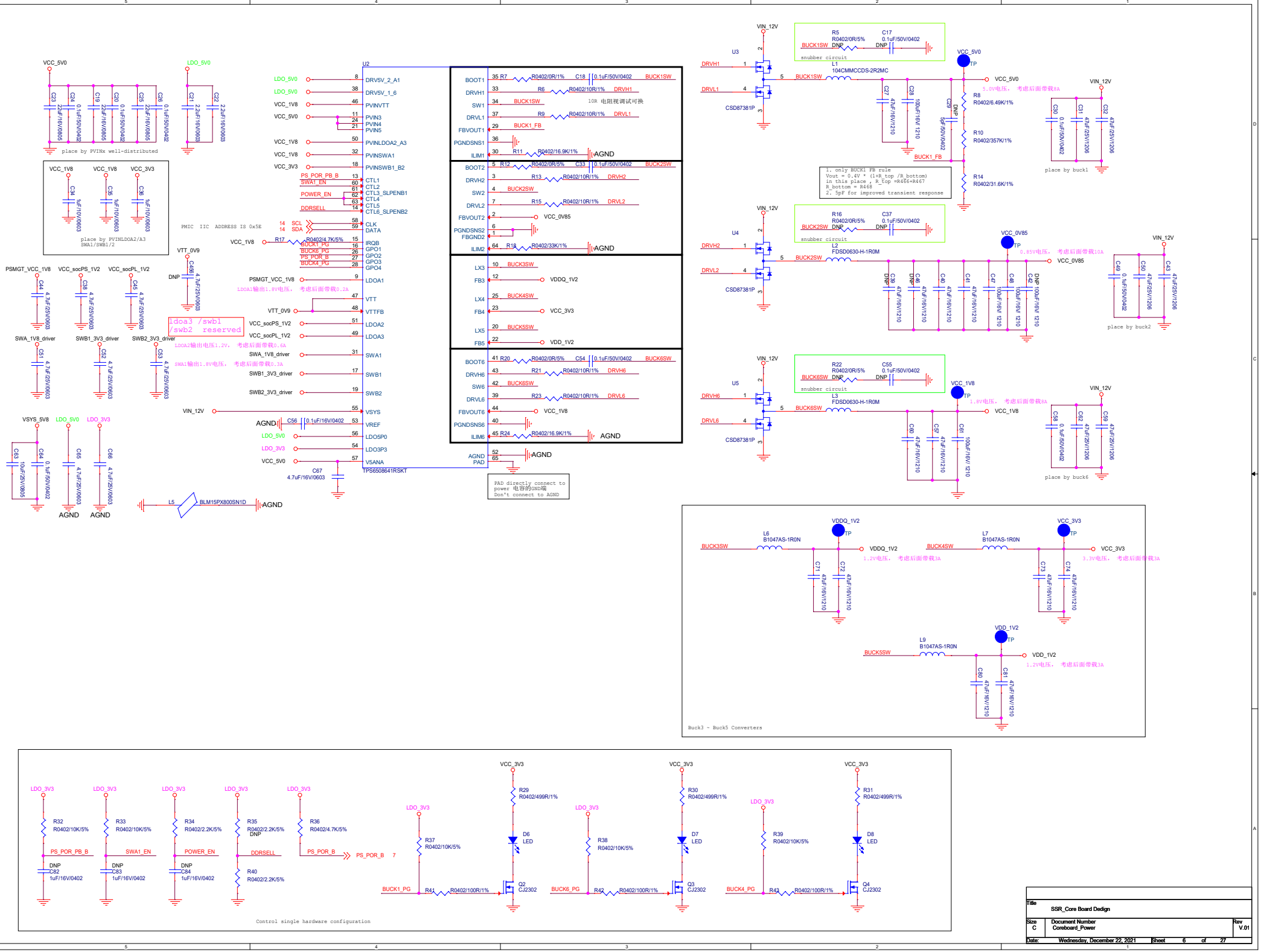
U2
TPS6508641RSKT
DRV5V_2_A1
DRV5V_1_6
PVINVTT
PVIN3
PVIN4
PVIN5
PVINLDOA2_A3
PVINSWA1
PVINSWB1_B2
CTL1
CTL2
CTL3_SLPENB1
CTL4
CTL5
CTL6_SLPENB2
CLK
DATA
IRQB
GPO1
GPO2
GPO3
GPO4
LDOA1
VTT
VTTFB
LDOA2
LDOA3
SWA1
SWB1
SWB2
VSYS
VREF
LDO5P0
LDO3P3
V5ANA
BOOT1
DRVH1
SW1
DRVL1
FBVOUT1
PGNDSNS1
ILIM1
BOOT2
DRVH2
SW2
DRVL2
FBVOUT2
PGNDSNS2
FBGND2
ILIM2
LX3
FB3
LX4
FB4
LX5
FB5
BOOT6
DRVH6
SW6
DRVL6
FBVOUT6
PGNDSNS6
ILIM6
AGND PAD
PAD directly connect to power 电容的GND脚
Don't connect to AGND
PMIC IIC ADDRESS IS 0x5E
ldoa3 /swb1 /swb2 reserved
LDOA1输出1.8V电压， 考虑后面带载0.2A
LDOA2输出电压1.2V， 考虑后面带载0.6A
SWA1输出1.8V电压， 考虑后面带载0.3A
place by PVINLDOA2/A3 SWA1/SWB1/2
place by PVINx well-distributed
L5 BLM15PX800SN1D
U3 CSD87381P
U4 CSD87381P
U5 CSD87381P
L1 104CMMCCDS-2R2MC
L2 FDSD0630-H-1R0M
L3 FDSD0630-H-1R0M
snubber circuit
VCC_5V0 5.0V电压， 考虑后面带载8A
VCC_0V85 0.85V电压， 考虑后面带载10A
VCC_1V8 1.8V电压， 考虑后面带载8A
place by buck1
place by buck2
place by buck6
1. only BUCK1 FB rule
Vout = 0.4V * (1+R_top /R_bottom)
in this place , R_top =R456+R467
R_bottom = R468
2. 5pF for improved transient response
L6 B1047AS-1R0N
L7 B1047AS-1R0N
L9 B1047AS-1R0N
VDDQ_1V2 1.2V电压， 考虑后面带载3A
VCC_3V3 3.3V电压， 考虑后面带载3A
VDD_1V2 1.2V电压， 考虑后面带载3A
Buck3 ~ Buck5 Converters
Control single hardware configuration
Title
SSR_Core Board Dedign
Size C
Document Number Coreboard_Power
Rev V.01
Date: Wednesday, December 22, 2021
Sheet 6 of 27