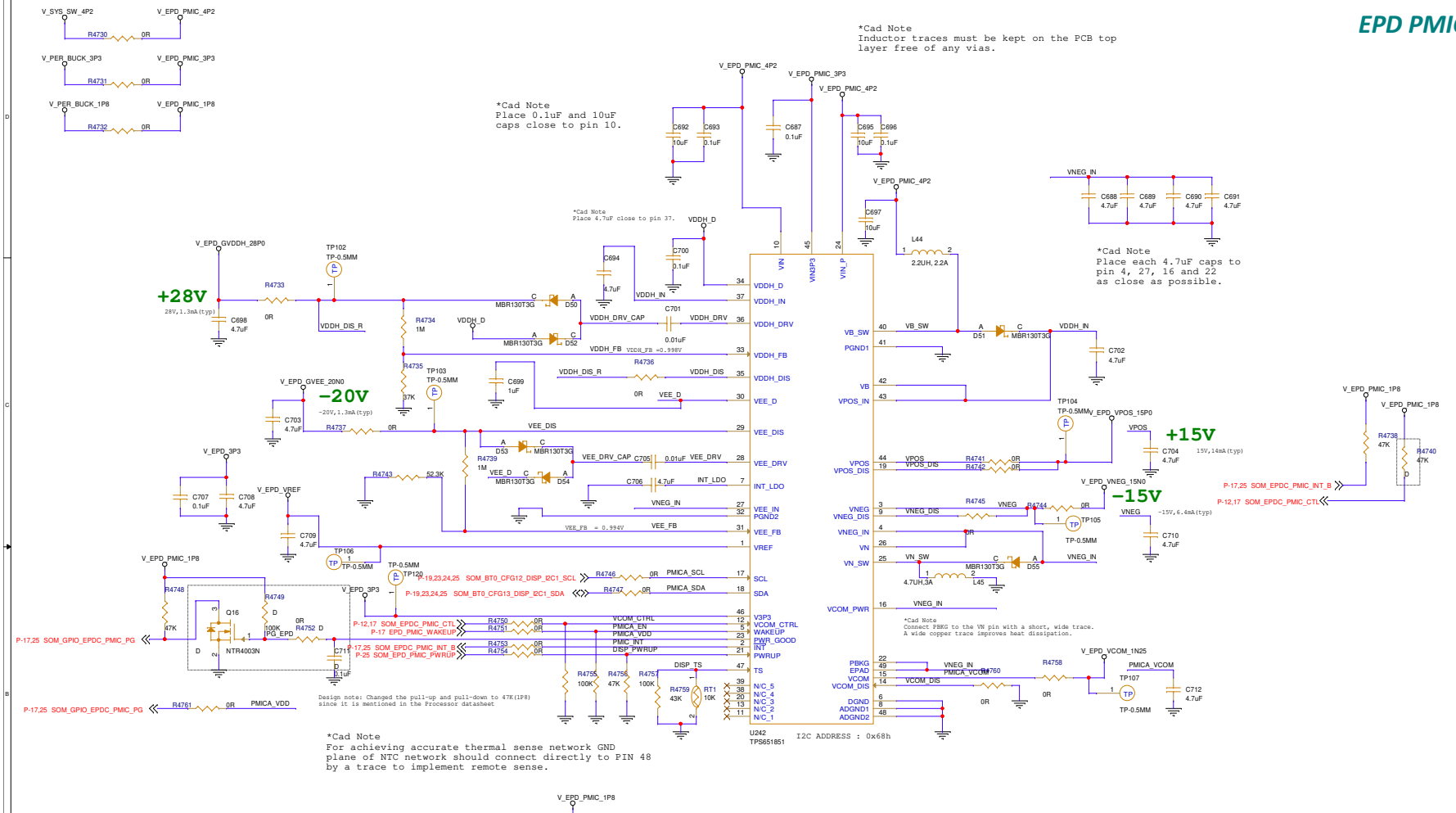
EPD PMIC


V_SYS_SW_4P2
V_EPD_PMIC_4P2
R4730 0R
V_PER_BUCK_3P3
V_EPD_PMIC_3P3
R4731 0R
V_PER_BUCK_1P8
V_EPD_PMIC_1P8
R4732 0R
*Cad Note
Inductor traces must be kept on the PCB top layer free of any vias.
*Cad Note
Place 0.1uF and 10uF caps close to pin 10.
*Cad Note
Place 4.7uF close to pin 37.
*Cad Note
Place each 4.7uF caps to pin 4, 27, 16 and 22 as close as possible.
+28V
28V,1.3mA(typ)
-20V
-20V,1.3mA(typ)
+15V
15V,14mA(typ)
-15V
-15V,6.4mA(typ)
VDDH_D
VDDH_IN
VDDH_DRV_CAP
VDDH_DRV
VDDH_FB
VDDH_FB =0.998V
VDDH_DIS_R
VDDH_DIS
VEE_D
VEE_DIS
VEE_DRV_CAP
VEE_DRV
INT_LDO
VNEG_IN
VEE_FB
VEE_FB = 0.994V
VREF
SCL
SDA
V3P3
VCOM_CTRL
WAKEUP
PWR_GOOD
INT
PWRUP
TS
N/C_5
N/C_4
N/C_3
N/C_2
N/C_1
VN
VIN3P3
VIN_P
VB_SW
PGND1
VB
VPOS_IN
VPOS
VPOS_DIS
VNEG
VNEG_DIS
VN
VN_SW
VCOM_PWR
PBKG
EPAD
VCOM
VCOM_DIS
DGND
ADGND1
ADGND2
U242
TPS651851
I2C ADDRESS : 0x68h
*Cad Note
Connect PBKG to the VN pin with a short, wide trace.
A wide copper trace improves heat dissipation.
*Cad Note
For achieving accurate thermal sense network GND plane of NTC network should connect directly to PIN 48 by a trace to implement remote sense.
Design note: Changed the pull-up and pull-down to 47K(1P8) since it is mentioned in the Processor datasheet
P-17,25 SOM_GPIO_EPDC_PMIC_PG
P-12,17 SOM_EPDC_PMIC_CTL
P-17 EPD_PMIC_WAKEUP
P-17,25 SOM_EPDC_PMIC_INT_B
P-25 SOM_EPD_PMIC_PWRUP
P-19,23,24,25 SOM_BT0_CFG12_DISP_I2C1_SCL
P-19,23,24,25 SOM_BT0_CFG13_DISP_I2C1_SDA
P-17,25 SOM_EPDC_PMIC_INT_B
P-12,17 SOM_EPDC_PMIC_CTL
PMIC WAKEUP SIGNAL
LOGIC INVERTER
EPD_PMIC_WAKEUP P-17
P-25 SOM_EPDC_PMIC_WAKEUP_B
DESIGNED BY Z-CROSSING SOLUTIONS
Title
EPD PMIC
Size C
Document Number
<Doc>
Rev A
Date: Sunday, December 08, 2024
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