

# TPS65200 APPLICATION REPORT

## Selecting CBOOT to avoid back-boost into VBUS

### Problem Description

The TPS65200 hosts a synchronous switching charger for single-cell Li+ batteries with input-voltage dynamic power management (VDPM). This feature reduces the battery charging current to maintain a minimum input voltage when the charge adapter is not capable of providing the full charging current. This feature makes the TPS65200 compatible with after-market and older wall adapters.

However, VDPM poses a challenge to the design when trying to detect that a wall adapter has been removed from the charger. In particular it can lead to 'back-boost', an operating condition where the charger operates in reverse direction, boosting the battery voltage to the VDPM voltage and delivering power to VBUS even after the charger adapter has been removed. This report describes the conditions that can lead to back-boost and provides a method of selecting the proper value of the boot-strap capacitor and VDPM regulation voltage to avoid 'back-boost'.

### Charger Description

Figure 1 shows a simplified block diagram of the switching charger. In normal operation  $V_{VBUS}$  is greater than  $V_{BAT}$  and the charger operates as a buck converter, delivering a constant current or constant voltage to the battery, depending on its state of charge. Q2 is a NMOS transistor and requires a gate-drive voltage greater than  $V_{BAT}$ . This voltage is provided by the boot-strap capacitor CBOOT. In each switching cycle CBOOT is charged to  $V_{VBUS}$  minus a diode forward-voltage  $V_f$  while Q3 is conducting, and charge is delivered to the gate driver of Q2 while Q3 is blocking and Q2 is conducting.

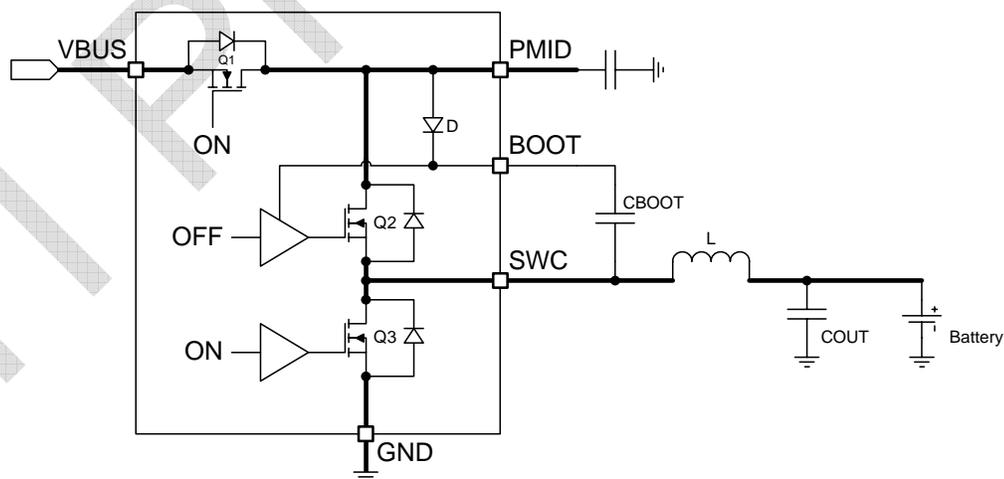
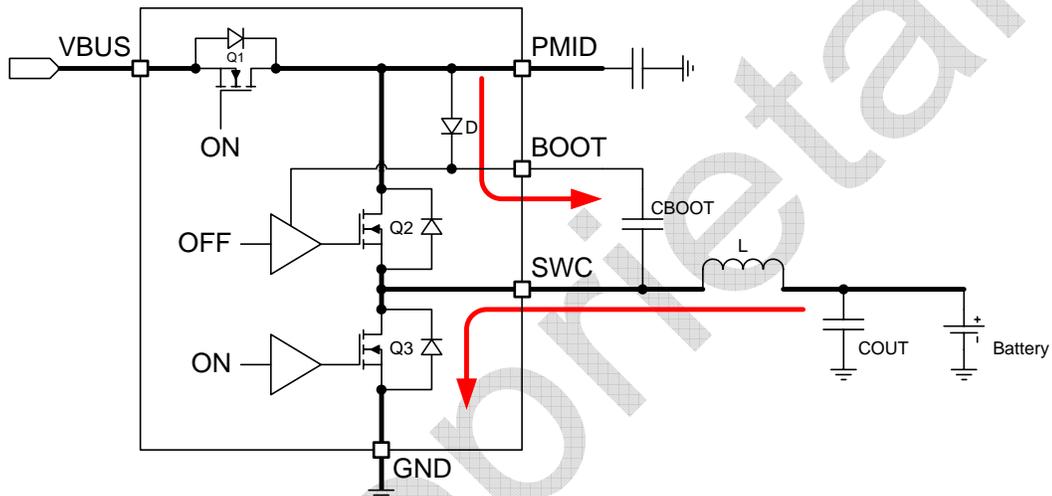


Figure 1: Simplified block diagram of switching charger

As the battery voltage increases, charging current is reduced together with the duty cycle of Q2: Q2 ON-time is shortened and Q3 ON-time is increased. At charging currents <math><100\text{mA}</math> Q3 is kept OFF and Q3's body diode is used for recirculation to avoid current reversal in the inductor L which could otherwise also cause a back-boost issue. With Q3 kept OFF, the boot-strap capacitor is not recharged and Q2 quickly loses gate drive. To avoid this, Q3 is turned ON for 40ns when CBOOT voltage drops below 2V to recharge the bootstrap capacitor.

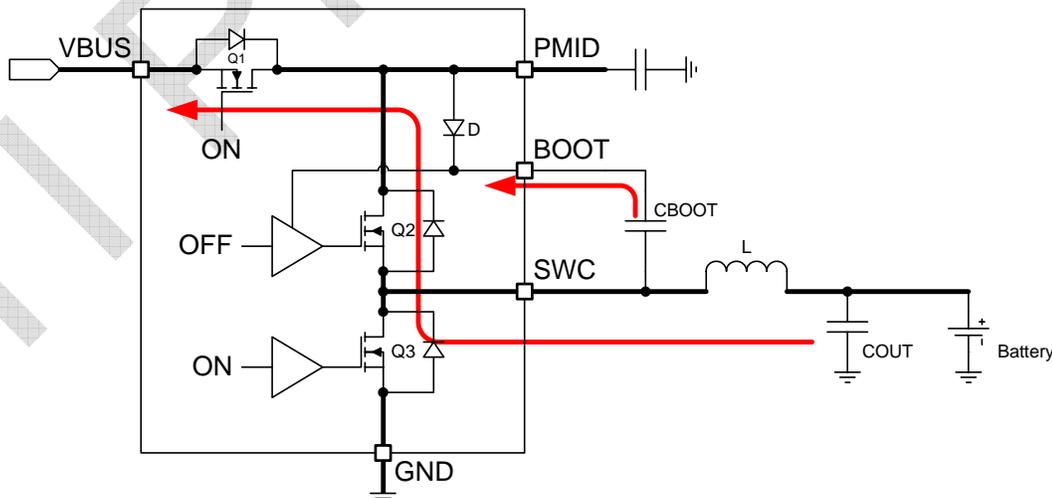
### Refreshing the boot-strap capacitor CBOOT

When the USB or wall adapter is removed during battery charging, the charger continues to provide current to the battery and as a result  $V_{VBUS}$  drops. When  $V_{VBUS}$  approaches the VDPM regulation voltage, the control loop reduces the charging current to near zero and as a result Q2 has a very short duty cycle and Q3 is held OFF with the exception of the 40ns refresh-pulses required to maintain voltage on CBOOT. During the 40ns ON-time of Q3, the current in inductor L reverses, flowing from the battery, through L and Q3 to ground as shown in Figure 2.



**Figure 2: Current flow during 40ns refresh pulse**

Next, when Q3 is turned back off, the energy stored in the inductor is delivered to VBUS through the body-diode of Q2. This is shown in Figure 3.



**Figure 3: Current flow immediately after the 40ns refresh pulse**

The frequency at which this happens depends on:

- The value of CBOOT. More charge is stored on a bigger capacitor and therefore it needs to be refreshed less frequently.
- The VDPM voltage. CBOOT is charged to  $(V_{VDPM} - V_f)$  where  $V_f$  is the forward voltage of diode D. The higher the VDPM voltage, the more charge is stored on CBOOT and the less frequently it needs to be refreshed.
- The amount of current pulled from CBOOT by the Q2 gate driver.
- The amount of leakage-current of CBOOT.

### Continuous back-boost condition

During two refresh pulses VBUS is discharged by whatever circuitry is connected internal to the IC. If the energy built up in the inductor during a refresh pulse is greater or equal to the energy pulled from VBUS in-between two refresh pulses, the charger will operate as a boost converter and maintain the VDPM voltage at VBUS. This condition is called back-boost and is an undesired mode of operation.

### Calculating the minimum boot-strap capacitor

The minimum energy that needs to be delivered to VBUS to maintain back-boost depends on:

- The discharge current on VBUS. Higher discharge current requires more energy delivered to VBUS.
- The battery and VDPM regulation voltage. Assuming an ideal Q2 body diode, VBUS is discharged from  $V_{VDPM}$  to  $V_{BAT}$  in-between two refresh cycles. The higher  $V_{VDPM}$  and the lower  $V_{BAT}$ , the more energy needs to be delivered to VBUS to maintain the back-boost condition.

The energy pulled from VBUS in-between two refresh cycles is given by:

$$(V_{VDPM} - V_{BAT}) \times I_{BUS} \times \tau \quad \text{Eq. (1)}$$

Where  $V_{VDPM}$  is the VDPM regulation voltage,  $V_{BAT}$  is the battery voltage,  $I_{BUS}$  is the discharge current on VBUS and  $\tau$  is the time in-between two refresh pulses.

The energy built-up in the inductor during a refresh-pulse is given by:

$$\frac{1}{2} L \times I^2 = \frac{1}{2L} \times V_{BAT}^2 \times t_{ON}^2 \quad \text{Eq. (2)}$$

Where L is the inductor value, I is the inductor peak-current, and  $t_{ON}$  is the refresh-pulse width (40ns).

To maintain back-boost, the energy built up in the inductor during a refresh-pulse needs to equal the energy pulled from VBUS in-between refresh pulses, therefore equation (1) needs to equal equation (2) and we can calculate  $\tau$  as:

$$\tau = \frac{t_{ON}^2 \times V_{BAT}^2}{2 \times L \times I_{BUS} \times (V_{VDPM} - V_{BAT})} \quad \text{Eq. (3)}$$

If the time in-between two refresh pulses exceeds  $\tau$ , back-boost cannot be maintained. In other words, the energy built-up in the inductor during refresh is less than the energy pulled from VBUS in-between refresh pulses. With this, we can now calculate the minimum value of the boot-strap capacitor. CBOOT must be capable of storing enough charge to supply the gate driver with current for  $>\tau$ , therefore  $C_{BOOT,MIN}$  can be calculated as:

$$C_{BOOT,MIN} = \frac{I_{DIS} \times \tau}{V_{VDPM} - V_f - V_{refresh}} \quad \text{Eq. (4)}$$

Where  $I_{DIS}$  is the discharge current of CBOOT,  $V_f$  is the forward voltage of diode D and  $V_{refresh}$  is the minimum voltage across CBOOT at which a refresh pulse is triggered.

### An example in numbers

The following section calculates the minimum CBOOT value required for reliable operation without back-boost. The following assumptions are made:

- The maximum battery voltage is 4.2V
- The VDPM voltage is 4.36V (TPS65200 default)
- The discharge current  $I_{BUS} = 2\text{mA}$  (a conservative estimate)
- The refresh pulse width  $t_{ON} = 40\text{ns}$  (a design parameter)
- The inductor value  $L = 1\mu\text{H}$
- The forward voltage of diode D  $V_f = 0.7\text{V}$
- The refresh voltage  $V_{refresh} = 2\text{V}$  (a design parameter)
- The discharge current of CBOOT is 1mA (experimentally confirmed value)

From equation (3) we calculate  $\tau = 44.1\mu\text{s}$  and from equation (4) we calculate  $C_{BOOT\_MIN} = 26.6\text{nF}$ . Allowing for 20% variation of the nominal capacitor value we choose a 33nF capacitor for CBOOT. To charge a 33nF capacitor in 40ns from 2V to (4.36V-0.7V) actually requires 1.4A of current. This is a large current and any series resistance to CBOOT will impact it's ability to be fully charged. Therefore a lower capacitor value is desirable.

From equation (3) and (4) it can be seen that a higher VDPM voltage will result in a smaller  $C_{BOOT\_MIN}$ . If VDPM is increased to 4.44V,  $\tau$  reduces to 29.4us and  $C_{BOOT\_MIN} = 16.9\text{nF}$ . We choose a 22nF capacitor and the CBOOT refresh current drops to <1A.

VBUS [V]	CBOOT = 10nF		CBOOT = 22nF		CBOOT = 33nF	
	$\tau$ [ms]	Peak Voltage [V]	$\tau$ [ms]	Peak Voltage [V]	$\tau$ [ms]	Peak Voltage [V]
5	1.60	8.16	2.86	7.80	3.7	7.48
4.8	1.44	7.97	2.57	7.68	3.35	7.38
4.6	1.27	7.78	2.25	7.54	2.98	7.28
4.4	1.10	7.6	1.92	7.40	2.58	7.17
4.2	0.82	7.4	1.58	7.24	2.13	7.06

**Table 1: Measurement results on boot-strap caps with different value showing the diminishing effect of larger boot-strap capacitors.  $\tau$  is expected to be proportional to CBOOT but measurements indicate that the 40ns recharge time and series resistance are limiting the amount of charge that is stored on the capacitor during re-fresh. The drop-off in peak voltage on BOOT pin is another indication that a 33nF capacitor cannot be fully charged.**

### Recovery from back-boost

When the switching charger is locked into back-boost it will draw current from the battery and slowly discharge the system. As the battery voltage drops, the energy stored in the inductor during the refresh pulse drops per equation (2) and eventually won't be sufficient to sustain back-boost. To calculate the battery voltage at which the system recovers from back-boost for a given boot-strap capacitor, we take equation (3) and (4) and solve for  $V_{BAT\_MIN}$ :

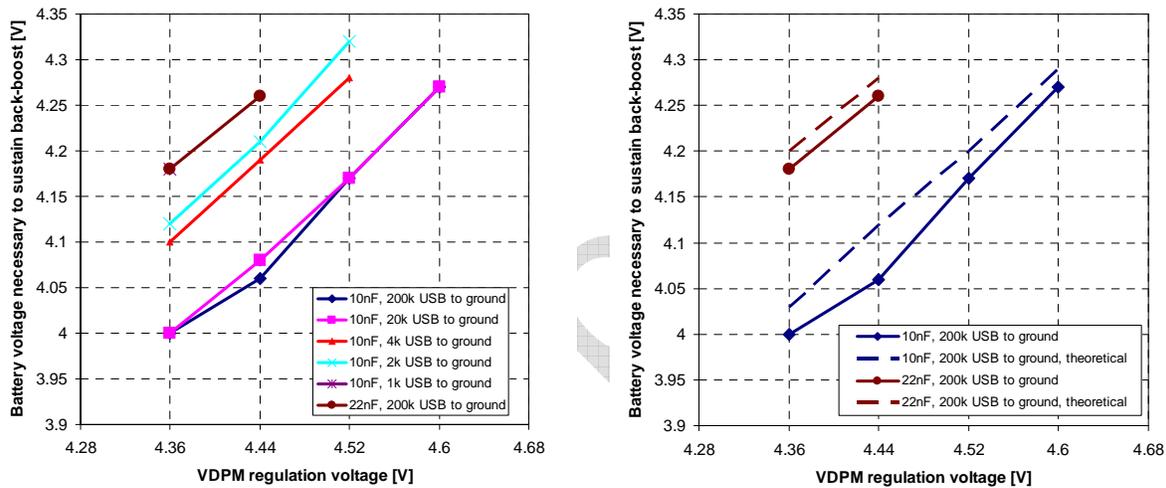
$$V_{BAT\_MIN} = \frac{-C_{BOOT} + \sqrt{C_{BOOT}^2 + 4 \times a \times C_{BOOT} \times V_{VDPM}}}{2 \times a} \quad \text{Eq. (5a)}$$

$$a = \frac{t_{ON}^2 \times I_{DIS}}{2 \times L \times I_{BUS} \times (V_{VDPM} - V_f - V_{refresh})} \quad \text{Eq. (5b)}$$

Let's assume:

- The VDPM voltage is 4.36V (TPS65200 default)
- CBOOT = 10nF
- The discharge current  $I_{BUS} = 2\text{mA}$  (a conservative estimate)
- The refresh pulse width  $t_{ON} = 40\text{ns}$  (a design parameter)
- The inductor value  $L = 1\mu\text{H}$
- The forward voltage of diode  $D V_f = 0.7\text{V}$
- The refresh voltage  $V_{refresh} = 2\text{V}$  (a design parameter)
- The discharge current of CBOOT is 1mA (experimentally confirmed value)

Then  $V_{BAT,MIN}$  is calculated as 3.98V. If CBOOT is 8nF (10nF-20%),  $V_{BAT,MIN}$  drops to 3.90V. Worst case the battery can be discharged to this value before back-boost stops.



**Figure 4: LEFT: Measurement of the minimum battery voltage required to sustain back-boost mode as a function of selected VDPM regulation voltage. With a 22nF boot-strap cap and VDPM voltage of 4.44V or higher back-boost cannot be sustained with battery voltage of 4.2V or less. RIGHT: A comparison between measurement results (solid lines) and theoretical calculations (dashed lines). Theory predicts the battery voltage within 40mV or better.**

## Summary

The boot-strap cap CBOOT must be carefully chosen to avoid back-boost into VBUS when the charger adapter is removed from VBUS. This report shows that a 10nF capacitor is not sufficient to avoid back-boost under all conditions. However, CBOOT cannot be increased without limits due to the fixed width of the refresh-pulse and concerns over the peak charge-current required to fully charge CBOOT. A good compromise is selecting a 22nF CBOOT and increasing the VDPM voltage to 4.44V. Experimental results confirm that this combination leads to reliable operation of the charger with out back-boost.

The equations also show that back-boost cannot be maintained for extended period of time. A worst-case calculation shows back-boost cannot be sustained below 3.9V battery voltage with a boot-strap cap of 8nF.