TPS6521920WRHBRQ1	Configuration Input Supply: 3.3V Processor: AM62Q Memory: LPDDR4		Notes
BUCK1	Vout	0.75 V	
	Bandwidth	High bandwidth	
	UV	5%	
BUCK2	Vout	1.8 V	
	Bandwidth	High bandwidth	
	UV	5%	
BUCK3	Vout	1.1 V	
	Bandwidth	High bandwidth	
	UV	5%	
Buck1/2/3 Switching Mode	Quasi-fixed frequency	converters can operate in **forced-PWM,** irrespective of load-current, or can be allowed to enter **pulse-frequency-modulation (PFM)** for low load-currents.	TPS65219-Q1 also offers fixed frequency mode (spread-spectrum available) but this configuration requires a new orderable.
LDO1	Vout	3.3 V / 1.8 V	LDO1 configured as bypass
	UV	5%	
LDO2	Vout	0.85 V	
	UV	5%	
LDO3	Vout	1.8 V	
	UV	5%	
LDO4	Vout	1.2 V	
	UV	5%	
GPIO	GPO1	Disabled	GPO1 can be enabled through I2C (optional)
	GPO2	Enabled	GPO2 will automatically be enabled during power-up
	GPIO	Disabled	GPIO can be enabled through I2C (optional)
MODE_RESET	Config	Warm reset	cold reset can be triggered through I2C
	Polarity	High= normal operation Low = warm reset	
MODE_STANDBY	Config	Standby	
	Polarity	High = ACTIVE State Low = STBY	TPS6521920W was configured to have all rails enabled in Active and Standby.
VSEL_SD/VSEL_DDR	Config	VSEL_SD	
	Rail controlled by VSEL_SD	LDO1	
	Polarity	High = VOUT register Low = 1.8 V	VSEL_SD=HIGH will set an output voltage of 3.3V on LDO1 (LDO1 behaves as bypass). VSEL_SD=LOW will set an output voltage of 1.8V on LDO1 (LDO1 behaves as LDO)
EN_PB_VSENSE	Config	Push-button	Holding the PB low for ~600ms will wake-up the PMIC.

			Holding PB low for ~8s will turn OFF the PMIC.
First Supply Detection (FSD)	Config	Enabled	This feature will ignore the state of the PB pin during the first power-up and PMIC will transition from “No Power” to “Active” when main supply is connected.

Example Block Diagram: