8.3.1	I_{OUT}	Output Current				300	mA
8.4.1	C_{IN}	Input Filtering Capacitance (2)		2.2	4.7		µF
8.4.2	C_{OUT}	Output Filtering Capacitance (2)	Connected from VLDOx to GND, LDO-mode	1.6	2.2	4	µF
8.4.3a	$C_{OUT\_TOTAL\_FAST}$	Total Capacitance at Output (Local + POL), fast ramp-time (3)	1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH			15	µF
8.4.3b	$C_{OUT\_TOTAL\_SLOW}$	Total Capacitance at Output (Local + POL), slow ramp-time (3)	1 MHz < f < 10 MHz, impedance between output and point-of-load maximum 6nH			30	µF

(3) Additional capacitance, including local and POL, beyond the specified value can cause the LDO to become unstable

7.5.6 LDO3_VOUT Register (Offset = 5h) [Reset = 00h]

LDO3_VOUT is shown in Figure 7-17 and described in Table 7-13.

Return to the Table 7-6.

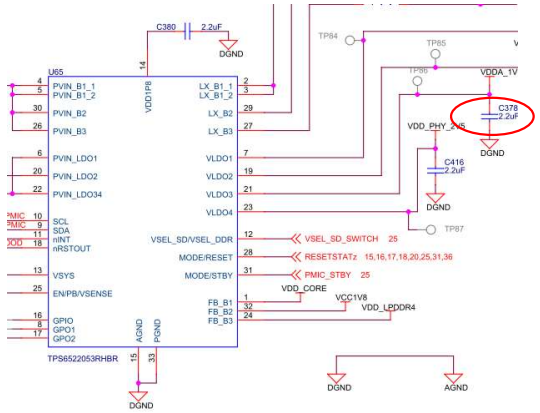
Figure 7-17. LDO3_VOUT Register

7	6	5	4	3	2	1	0
LDO3_SLOW_PU_RAMP	LDO3_LSW_CONFIG	LDO3_VSET					
R/W-0h	R/W-0h	R/W-0h					

Table 7-13. LDO3_VOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LDO3_SLOW_PU_RAMP	R/W	0h	LDO3 Power-up ramp When set high, slows down the power-up ramp to ~3ms. Cout max 30uF When set low, ramp time is ~660us. Cout max 15uF (Default from NVM memory) 0h = Fast ramp for power-up (~660us) 1h = Slow ramp for power-up (~3ms)
6	LDO3_LSW_CONFIG	R/W	0h	LDO3 LDO or LSW Mode. !!! NOTE: ONLY CHANGE WHILE RAIL IS DISABLED !!! (Default from NVM memory) 0h = LDO Mode 1h = LSW Mode

Cout_local=2.2uF



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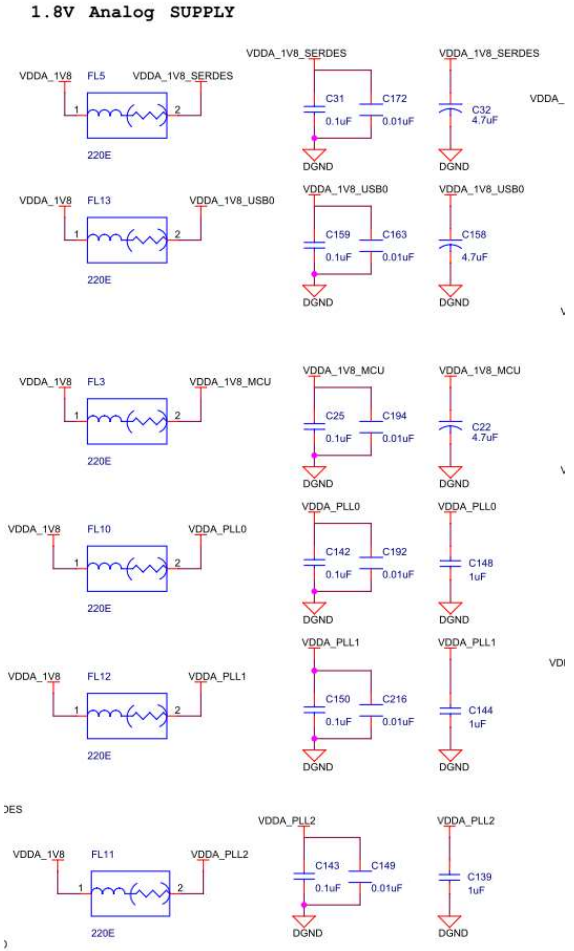

Cout_pol=4.7uFx3+1uFx3=17.1uF

Cout_total=19.3uF