VCC_2V5_DDR is our reference voltage for our expected voltage sequencing with respect to the outputs of TPS65262 Synchronous Buck converter

<u>Part No:</u> TPS65262-2RHBT
<u>Note:</u> Design Schematics attached below

<u>Observation 1:</u> C197 is mounted with 8.2nF at the pin SS1 [Pin 22]

Figure 1: VCCO_PSDDR_504 is generated from Buck 1 at LX1 [Pin 26] is 1.2V

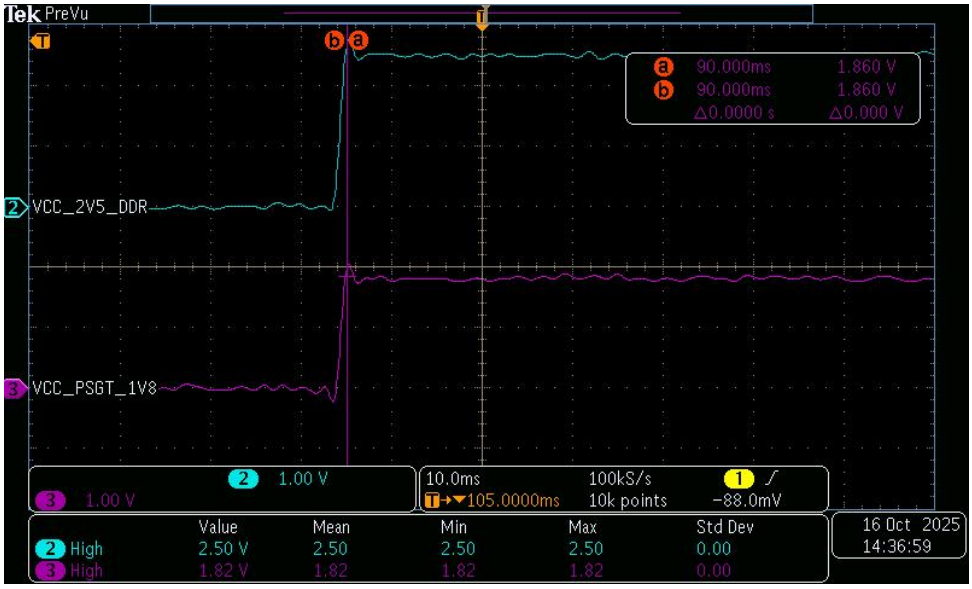

Figure 2: VCC_PSGT_1V8 is generated from LDO1 at LOUT1 [Pin 31] is 1.8V

Here, there is no delay in power up sequence of both the output voltage from LDO 1 output and Buck 1 output of TPS65262 with respect to reference voltage VCC_2V5_DDR

<u>Observation 2:</u> C197 is now mounted with 10nF at the pin SS1 [Pin 22]

Figure 3: VCCO_PSDDR_504 is generated from Buck 1 at LX1 [Pin 26] is 1.2V

Figure 4: VCC_PSGT_1V8 is generated from LDO1 at LOUT1 [Pin 31] is 1.8V

Here, we can see that there is an expected delay of 1.2ms for output of Buck 1 of TPS65262 with respect to the reference voltage VCC_2V5_DDR.
But, we are unable to provide any delay for LDO 1 output of the TPS65262 regulator as we expected a 1.2ms delay for Buck 1 ouptut after changing the capacitor from 8.2nF to 10nF

Required resolution on:

1. What is to be done for the delay to be added for LDO 1 output?
2. Is the behaviour correct for 8.2nF and 10nF for Buck 1 and LDO 1 output?

Attached design schematics for your reference below: