TPS65910 User Guide For OMAPL-137, OMAPL-138, and TMS320C674x Family of Processors

This user guide can be used as a reference for connectivity between the TPS65910 power-management integrated circuit (PMIC) and TI OMAPL, TMS320C674x processors.

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1 Introduction

This user guide can be used as a reference for connectivity between the TPS65910 PMIC and TI OMAPL, TMS320C674x processors. This user guide does not provide details about the power resources or the functionality of the device. For such information, refer to the full specification document, *TPS65910 Data Manual*.

2 Platform Connection

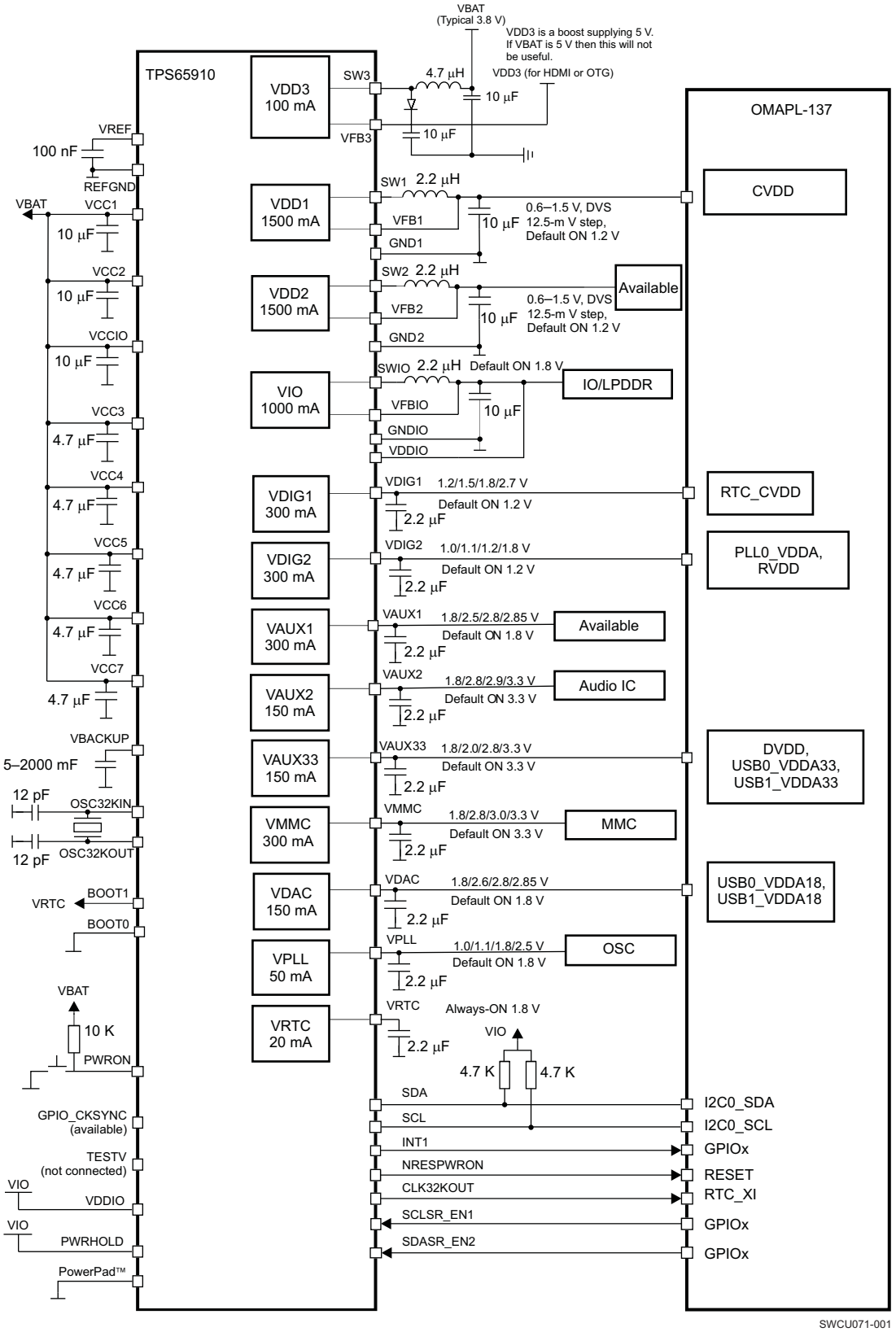
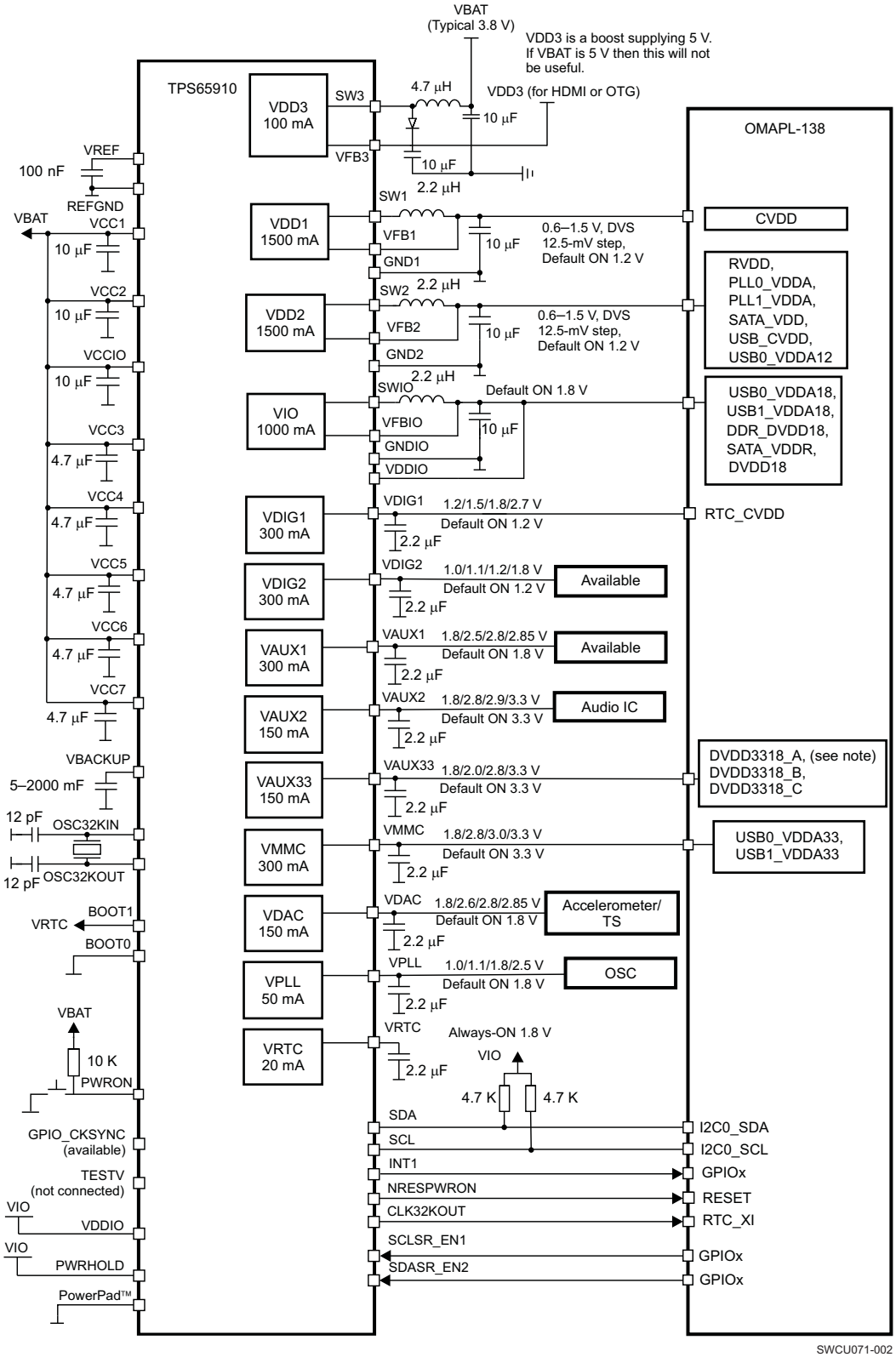


Figure 1. OMAPL-137 Power Supply Connections With TPS65910



NOTE: If only 1.8 V operation is required, then these domains can be merged with 1.8 V on VIO.

Figure 2. OMAPL-138, TMS320C6742/6/8 Power Connections With TPS65910

At power up, the maximum current capability (default setting) of the DCDC converters is as follows:

- VIO(max) = 500 mA
- VDD1(max) = 1000 mA
- VDD2(max) = 1000 mA

To have the maximum current capability, the user must program the following register bits:

- VIO_REG[ILMAX] = b01 for 1 A
- VDD1_REG[ILMAX] = b1 for 1.5 A
- VDD2_REG[ILMAX] = b1 for 1.5 A

3 Power-Up Sequencing

3.1 Power-Up Sequence for OMAPL-138 and TMS320C6742/6/8 Processors

The following sections show the power-up sequence requirement for OMAPL-138 and TMS320C6742/6/8 processors. To power on the system, the user must press and release the PWRON switch (generating a negative pulse). The BOOT pads on the TPS65910 must be connected as follows:

- BOOT0 = 0
- BOOT1 = 1

Table 1 lists the power rail requirements for OMAPL-138, TMS320C6742/6/8.

Table 1. Power Rail Requirements for OMAPL-138, TMS320C6742/6/8

Power Domain	Pin Name	I_{max} (mA)	Voltage (V)	Sequence
I/O	RTC_CVDD	1	1.2	1(1)
Core	CVDD(2)	600	1.0/1.1/1.2	2
I/O	RVDD, PLL0_VDDA, PLL1_VDDA, SATA_VDD, USB_CVDD, USB0_VDDA12	200	1.2	3
I/O	USB0_VDDA18, USB1_VDDA18, DDR_DVDD18, SATA_VDDR, DVDD18	180	1.8	4
I/O	USB0_VDDA33, USB1_VDDA33(3)(4)	24	3.3	5
I/O	DVDD3318_A, DVDD3318_B, DVDD3318_C	90(5)	3.3	5

(1) If RTC is not used/maintained on a separate supply, it can be included in the STATIC12 (fixed 1.2 V) group.

(2) If using CVDD at fixed 1.2 V, all 1.2-V rails may be combined. CVDD can support 1.3 V; in this case SMPS (VDD1) supplying CVDD core can be set to 1.3-V after initial power up.

(3) If 1.8-V LVCMOS is used, power rails up with the 1.8-V rails. If 3.3-V LVCMOS is used, power it up with the ANALOG33 rails (VDDA33_USB0/1).

(4) There is no specific required voltage ramp rate for any of the supplies LVCMOS33 (USB0_VDDA33, USB1_VDDA33) that never exceeds STATIC18 by more than 2 V.

(5) If DVDD3318_A, B, and C are powered independently, maximum power for each rail will be 1/3 the above maximum power. These rails can be connected independently to 1.8 or 3.3 V.

3.2 Power-Up Sequence for OMAPL-137 Processor

Table 2 lists the power rail requirements for OMAPL-137.

Table 2. Power Rail Requirements for OMAPL-137

Power Domain	Pin Name	I_{max} (mA)	Voltage (V) (2)	Sequence
Core	RTC_CVDD(1)	0.1	1.2	1
	CVDD	600	1.2	2
	PLL0_VDDA, RVDD	60	1.2	3
I/O	USB0_VDDA18, USB1_VDDA18	50	1.8	5
I/O	DVDD, USB0VDDA33, USB1_VDDA33	115	3.3	4

(1) RTC_CVDD can be combined with PLL and RAM 1.2-V supplies if desired to turn off RTC when device is off. Otherwise, power RTC_CVDD separately with a dedicated power source.

(2) Sequencing 1.2-V supplies:

(a) RTC (RTC_CVDD) may be powered from an external device (such as a battery) before all other supplies are applied. If the RTC is not used, RTC_CVDD must be connected to CVDD.
(b) Group 2a: CVDD core logic supply. CVDD can support 1.3 V, in this case SMPS (VDD1) supplying CVDD core can be set to 1.3 V after initial power up.
(c) Group 2b: Other 1.2-V logic supplies (RVDD, PLL0_VDDA). Groups 2a and 2b may be powered up together or 2a first followed by 2b.

NOTE: To correctly power on the device, the PWRHOLD signal must be high after PWRON is pressed. In this configuration the PWRHOLD signal on TPS65910 is connected to VIO. PWRHOLD transitions to high when VIO powers up.

3.3 Power-Up Sequence for TPS65910

To satisfy the power-up requirements for the OMAPL-138 and TMS320C6742/4/6 processors, the TPS65910 powers up with the default sequence when in the EEPROM boot mode configuration (BOOT0 = 0 and BOOT1 = 1) (see Table 3). The correct power-up sequence is configured in the EEPROM (factory programmable only).

Apart from the main power rails required by the processors, all other rails are also powered up at initial power up to support other system peripherals.

Figure 3 shows a typical power-up timing diagram.

Table 3 shows the power-up sequence.

Table 3. Power-Up Sequence for TPS65910

TPS65910 Power Rail	Voltage (V)	Sequence Number	Delay (ms)
PWRON(1)	–	–	
VDIG1	1.2	1	2
VDD1	1.2	2	2
VDD2	1.2	3	2
VIO	1.8	4	2
VDIG2	1.2	4	0
VAUX33	3.3	5	2
VMMC	3.3	5	0
VAUX1	1.8	6	2
VAUX2	3.3	6	0
VDAC	1.8	7	2
VPLL	1.8	7	0

(1) The PWRON signal is the start-on event. All timings listed are with respect to the previous event.

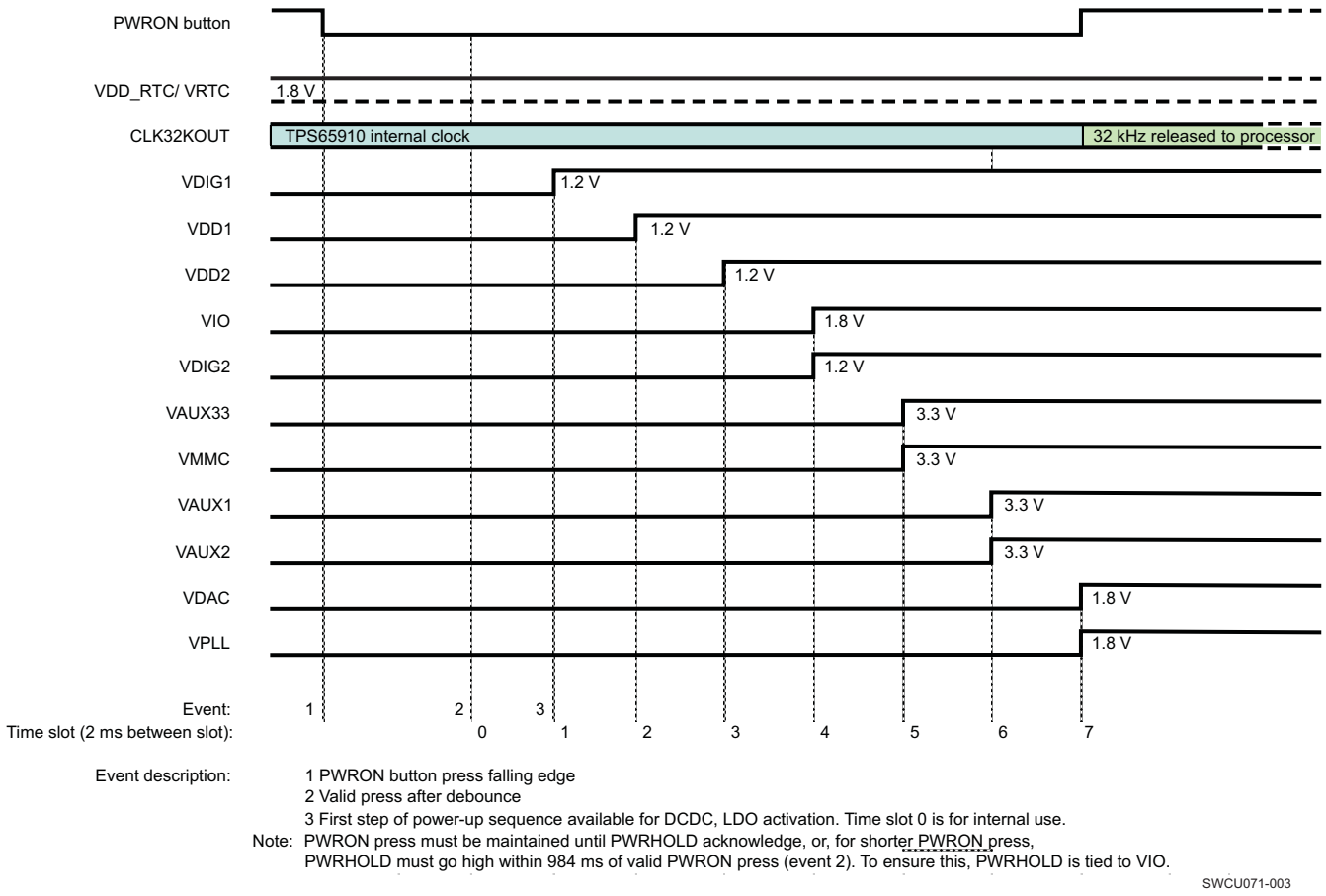


Figure 3. Power-Up Timing Diagram

Table 4. EEPROM Configuration for TPS65910

Register	Bit	Description	Option Selected
VDD1_OP_REG	SEL	VDD1 voltage level selection for boot	1.2 V
VDD1_REG	VGAIN_SEL	VDD1 gain selection, x1 or x2	x1
EEPROM		VDD1 time slot selection	2
DCDCCTRL_REG	VDD1_PSKIP	VDD1 pulse skip mode enable	Skip enabled
VDD2_OP_REG / VDD2_SR_REG	SEL	VDD2 voltage level selection for boot	1.2 V
VDD2_REG	VGAIN_SEL	VDD2 gain selection, x1 or x3	x1
EEPROM		VDD2 time slot selection	3
DCDCCTRL_REG	VDD2_PSKIP	VDD2 pulse skip mode enable	Skip enabled
VIO_REG	SEL	VIO voltage selection	1.8 V
EEPROM		VIO time slot selection	4
DCDCCTRL_REG	VIO_PSKIP	VIO pulse skip mode enable	Skip enabled
EEPROM		VDD3 time slot	OFF
VDIG1_REG	SEL	LDO voltage selection	1.2
EEPROM		LDO time slot	1
VDIG2_REG	SEL	LDO voltage selection	1.2 V
EEPROM		LDO time slot	4
VDAC_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	7

Table 4. EEPROM Configuration for TPS65910 (continued)

Register	Bit	Description	Option Selected
VPLL_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	7
VAUX1_REG	SEL	LDO voltage selection	1.8 V
EEPROM		LDO time slot	6
VMMC_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	5
VAUX33_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	5
VAUX2_REG	SEL	LDO voltage selection	3.3 V
EEPROM		LDO time slot	6
CLK32KOUT pin		CLK32KOUT time slot	7
NRESPWRON pin		NRESPWRON time slot	7 + 1
VRTC_REG	VRTC_OFFMASK	0 = VRTC LDO will be in low-power mode during OFF state. 1 = VRC LDO will be in full-power mode during OFF state.	Low-power mode
DEVCTRL_REG	RTC_PWDN	0 = RTC in normal power mode 1 = Clock gating of RTC register and logic, low-power mode	1
DEVCTRL_REG	CK32K_CTRL	0 = Clock source is crystal/external clock. 1 = Clock source is internal RC oscillator.	Crystal
DEVCTRL2_REG	TSLOT_LENGTH	Boot sequence time slot duration: 0 = 0.5 ms 1 = 2 ms	2 ms
DEVCTRL2_REG	IT_POL	0 = INT1 signal will be active low. 1 = INT1 signal will be active high.	Active low
INT_MSK_REG	VMBHI_IT_MSK	0 = Device automatically switches on at NO SUPPLY-to-OFF or BACKUP-to-OFF transition. 1 = Start-up reason is required before switch-on.	0 = Automatic switch on from supply insertion
VMBCH_REG	VMBCH_SEL[1:0]	Select threshold for main battery comparator threshold VMBCH.	3 V

4 Getting Started With TPS65910 and OMAPL-137, OMAPL-138, and TMS320C6742/6/8 Processors

4.1 First Initialization

4.1.1 I/O Polarity/Muxing Configuration

Program DEVCTRL2_REG.SLEEPSIG_POL according to the GPIO from the processor. This can be set to active low or active high for SLEEP transition. Software configuration allows specific power resources to enter low consumption state.

Set DEVCTRL_REG.DEV_SLP = 1 to allow SLEEP transition when requested.

Update the GPIO0 configuration (GPIO0_REG) based on your needs.

4.1.2 Define Wake-Up/Interrupt Event (SLEEP or OFF)

Select the appropriate bits in the INT_MSK_REG and INT_MSK2_REG registers to activate an interrupt to the processor on the INT1 line.

4.1.3 Backup Battery Configuration

If the system has a backup battery, set the BBCHEN bit to 1 in the BBCH_REG register, to enable backup battery charging. The maximum voltage to which the backup battery is charged is set by the BBSEL bits.

4.1.4 DCDC and Voltage Scaling Resource Configuration

Set DEVCTRL_REG[SR_CTL_I2C_REG] = 1 to control register using the control I^2C interface. Using the SCLSR_EN1 and SDASR_EN2 signals, the user can control the power resources. For OMAPL series, the following example is provided:

- SMPS control:
  - Configure two operating voltages for DCDC1 and DCDC2:
    - VDDx_OP_REG.SEL= Roof voltage (ENx ball high)
    - VDDx_SR_REG.SEL = Floor voltage (ENx ball low)
  - Assign control for VDD1 to SCLSR_EN1:
    - Set EN1_SMPS_ASS_REG.VDD1_EN1 = 1
    - Set SLEEP_KEEP_RES_ON_REG.VDD1_KEEPON = 1 (allow low-power mode)
- LDO control:
  - Assign control for VMMC regulator (for example, can be used for any other set of registers).
  - Set EN2_LDO_ASS_REG.VMMC_EN2 = 1
  - When SDASR_EN2 control signal is high then the regulator output depends on SLEEP_KEEP_LDO_ON setting.
  - SDASR_EN2 = 1, VMMC status is active.
  - SDASR_EN2 = 0 then:
    - SLEEP_KEEP_LDO_ON[VMMC_KEEPON] = 0, VMMC output is off.
    - SLEEP_KEEP_LDO_ON[VMMC_KEEPON] = 1, VMMC output is on in LOW-POWER state.

4.1.5 Sleep Platform Configuration

Configure the state of the LDOs when the SLEEP signal is used (by default all resources go into SLEEP state; in SLEEP state the LDO voltage is maintained but transient and load capability are reduced).

Resources that must provide full load capability must be set in the SLEEP_KEEP_LDO_ON_REG register.

Resources that can be set off in SLEEP state to optimize power consumption must be set in the SLEEP_SET_LDO_OFF_REG register.

4.2 Event Management Through Interrupts

4.2.1 INT_STS_REG.VMBHI_IT

INT_STS_REG.VMBHI_IT indicates that the supply (VBAT) is connected (leaving the BACKUP or NO SUPPLY state), the system must be initialized. (See Section 4.1, *First Initialization*.)

4.2.2 INT_STS_REG.PWRON_IT

INT_STS_REG.PWRON_IT is triggered when the PWRON button is pressed. If device is in OFF or SLEEP state, then this acts as a wake-up event and resources are reinitialized.

4.2.3 INT_STS_REG.PWRON_LP_IT

INT_STS_REG.PWRON_LP_IT is the PWRON long-press interrupt. This interrupt is generated when the PWRON button is pressed for 6 seconds. The application processor can make a decision to acknowledge the interrupt. If this interrupt is not acknowledged in the next 2 seconds then the device interprets this as a power-down event.

4.2.4 INT_STS_REG.HOTDIE_IT

INT_STS_REG.HOTDIE_IT indicates that the temperature of die is reaching the limit. Software must take action to decrease the power consumption before automatic shutdown.

4.2.5 INT_STS_REG.VMBDCH_IT

INT_STS_REG.VMBDCH_IT idicates that the input supply is low and the processor must prepare a shutdown to prevent losing data. This interrupt is linked to VBAT but does not apply to a system where PMIC is connect to 5-V rails and not directly to VBAT.

4.2.6 INT_STS2_REG.GPIO_R/F_IT

INT_STS2_REG.GPIO_R/F_IT is the GPIO interrupt event and can be used to wake up the device from SLEEP state. This can be an interrupt coming from any peripheral device or alike.

NOTE: This wake-up event is not valid for a transition from OFF state.

4.2.7 INT_STS_REG. RTC_ALARM_IT

INT_STS_REG. RTC_ALARM_IT is triggered when the RTC alarm set time is reached.

5 Revision History

Table 5. REVISION HISTORY

Version	Literature Number	Date	Notes
*	SWCU071	December 2010	See (1).
A	SWCS071A	July 2011	See (2).

(1) *TPS65910 User Guide For OMAPL-137, OMAPL-138, and TMS320C674x*, SWCU071 - Initial release.

(2) *TPS65910 User Guide For OMAPL-137, OMAPL-138, and TMS320C674x*, SWCU071A:
- Update Table 3: Change VAUX1 from 3.3 V to 1.8 V.

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