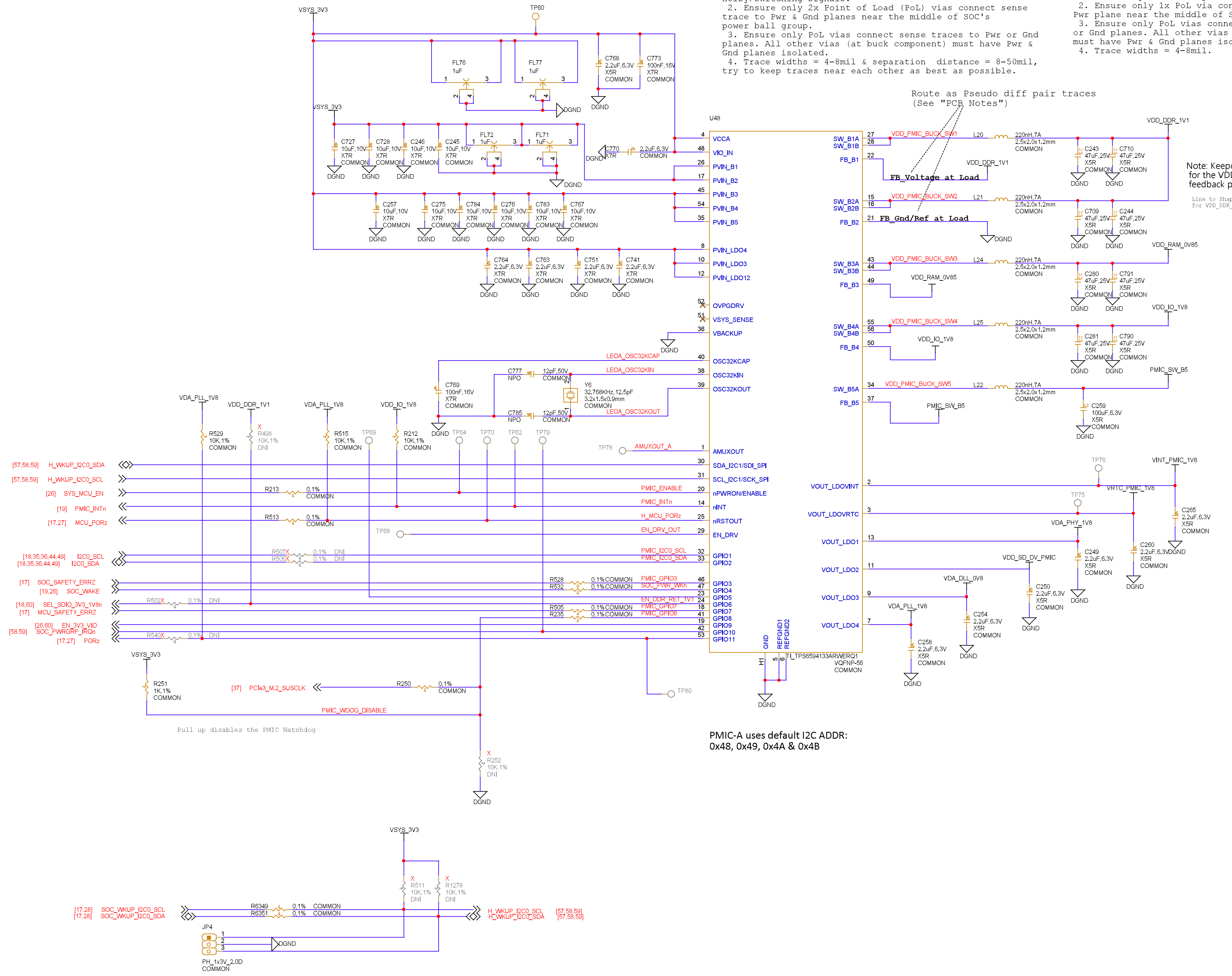
PMIC

"PCB Notes":
For multi-phase Buck converter configs, route remote sense feedback as follows:
1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:
1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
4. Trace widths = 4-8mil.



Note: Keepout needs to be provided for the VDD_DDR_1V1 and Gnd vias of the feedback pins connecting to the PMIC.

Line to Shape keepout needs to be given in layout for VDD_DDR_1V1 and DGND feedback traces

PMIC-A uses default I2C ADDR:
0x48, 0x49, 0x4A & 0x4B

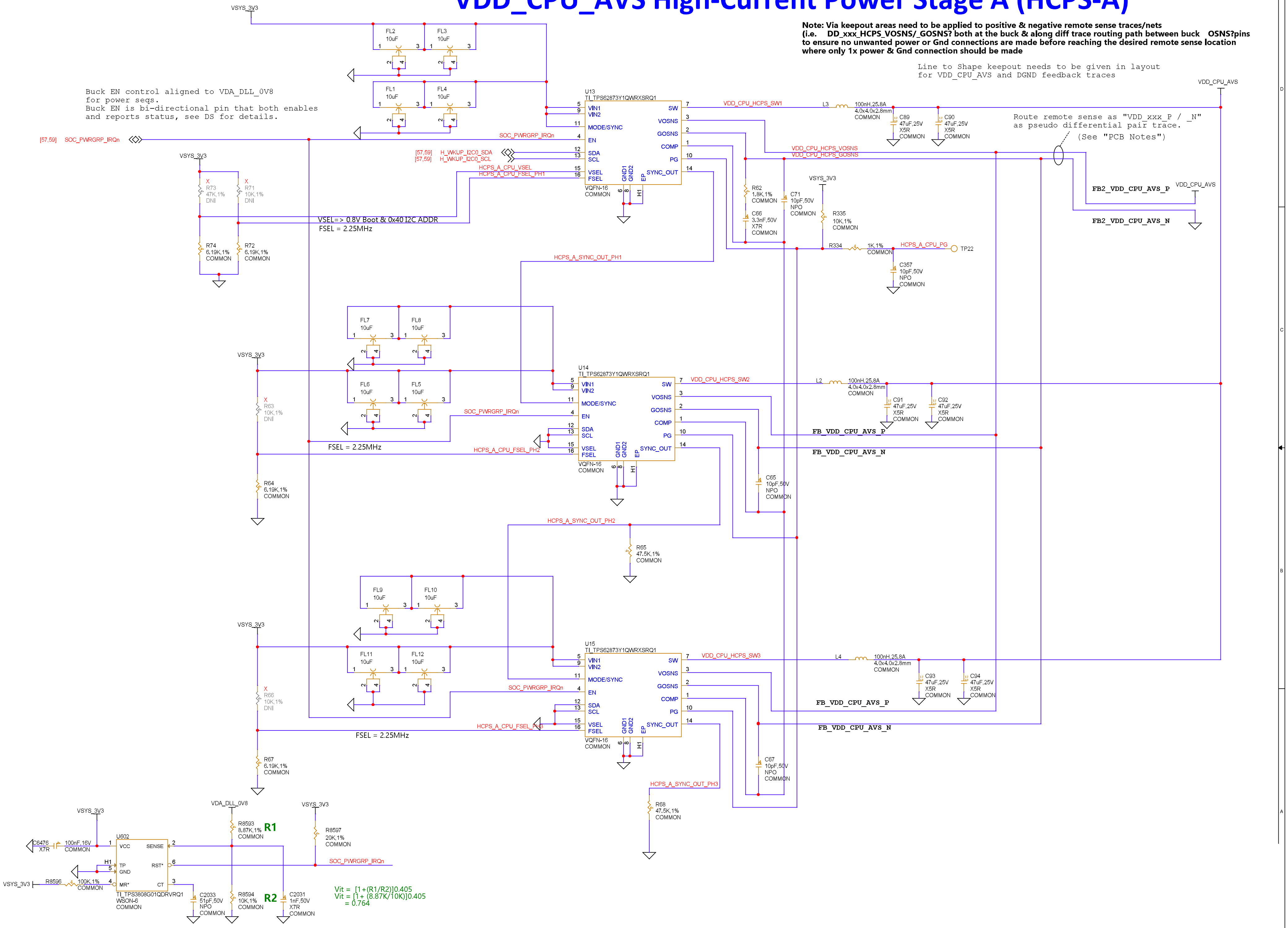
VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. DD_xxx_HCPS_VOSNS/_GOSNS? both at the buck & along diff trace routing path between buck OSNS?pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

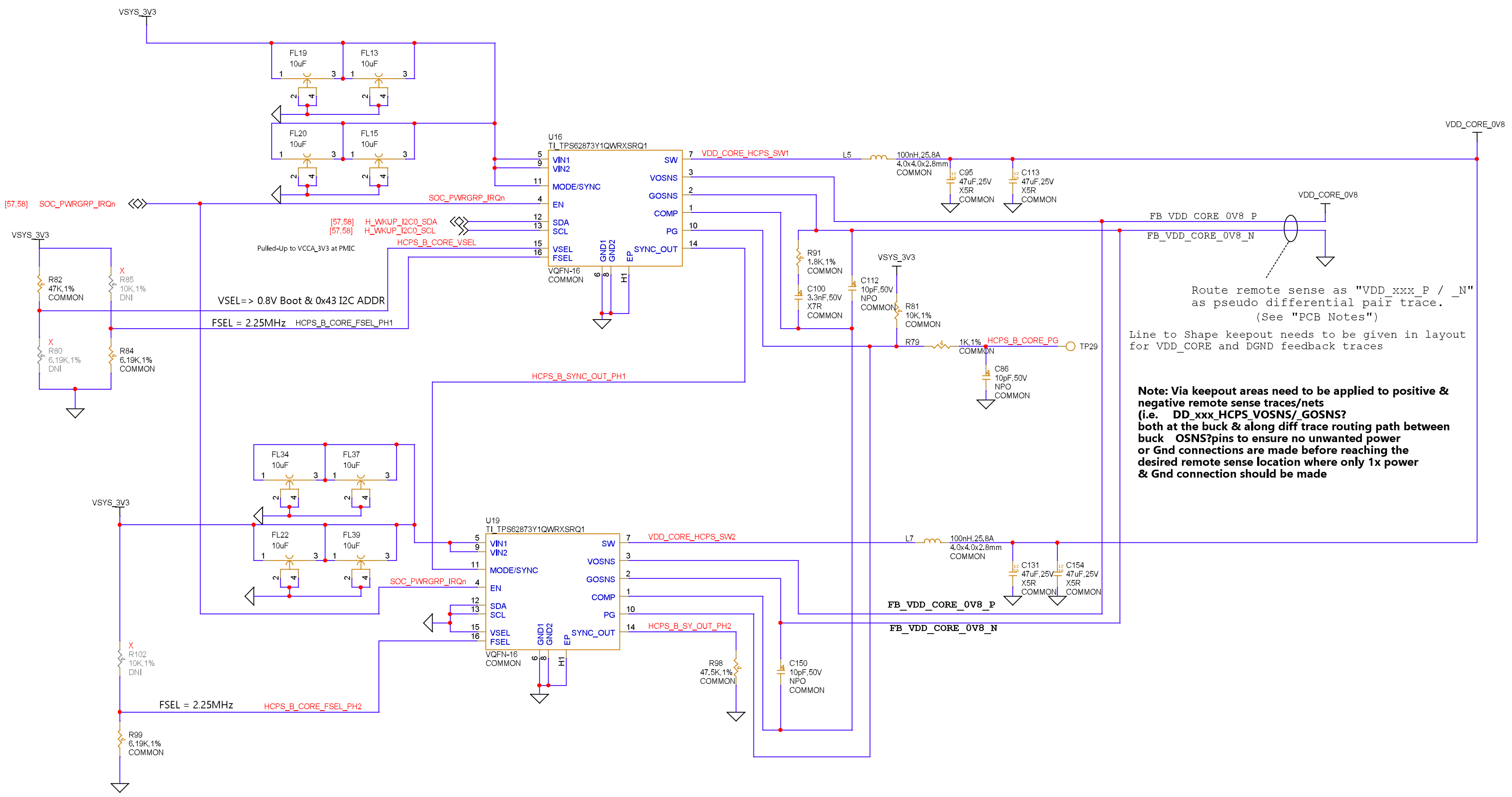
Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

Route remote sense as "VDD_xxx_P / _N" as pseudo differential pair trace. (See "PCB Notes")

Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.



VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



Route remote sense as "VDD_xxx_P / _N" as pseudo differential pair trace. (See "PCB Notes")

Line to Shape keepout needs to be given in layout for VDD_CORE and DGND feedback traces

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. DD_xxx_HCPS_VOSNS/_GOSNS? both at the buck & along diff trace routing path between buck OSNS?pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made