Desired Behavior: When a sink PD contract is negotiated, close the power path. If a type-C default contract, leave the power path open.

Suggested Fixes:

1) EC control using 'SRDy'

The TPS65987D can be configured to not enable the sink power path until an 'SRDY' Message is sent. In this case, you could use an MCU/EC to monitor the plug status of the TPS65987D, and on a new sink contract, check the contract negotiated. If it is a contract that you desire (a PD contract), your EC would send an 'SRDY' 4CC command to close the sink power path.

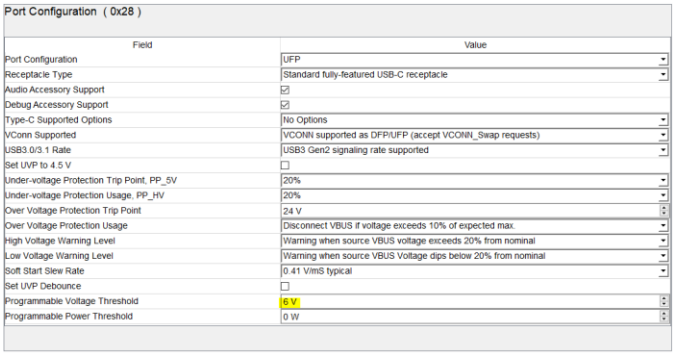
2) Potential Workaround: There may be a way to enable this behavior with native GPIO and configuration capabilities. This will require some testing on your end and some HW changes

We need 2 main things: (1) indicator that we are in a PD contract and (2) a way to disable/enable the power path.

(1) There is not single GPIO that exhibits this behavior. What we can do is use a combination of two GPIO events.

(a) Use the "Port 0 Sink Greater Than Threshold Event" to trigger any Contracts above a certain voltage. We can set the threshold in the Threshold voltage field of the Port Config register. Because the default USB-C contract and the PDO_0 contract have the same voltage, if we set the threshold below 5-V it would trigger for both and not behave as intended.

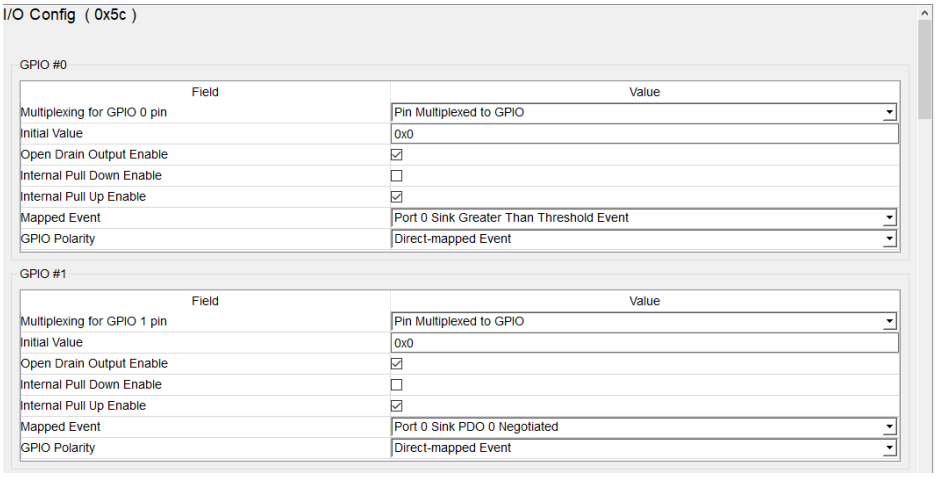
In this case, set it to a value > 5 and < 9, and it will cover all of the high voltage PD contracts.


Port Configuration (0x28)

Field	Value
Port Configuration	UFP
Receptacle Type	Standard fully-featured USB-C receptacle
Audio Accessory Support	☑
Debug Accessory Support	☑
Type-C Supported Options	No Options
VConn Supported	VCONN supported as DFP/UFP (accept VCONN_Swap requests)
USB3.0/3.1 Rate	USB3 Gen2 signaling rate supported
Set UVP to 4.5 V	☐
Under-voltage Protection Trip Point, PP_5V	20%
Under-voltage Protection Usage, PP_HV	20%
Over Voltage Protection Trip Point	24 V
Over Voltage Protection Usage	Disconnect VBUS if voltage exceeds 10% of expected max.
High Voltage Warning Level	Warning when source VBUS voltage exceeds 20% from nominal
Low Voltage Warning Level	Warning when source VBUS Voltage dips below 20% from nominal
Soft Start Slew Rate	0.41 V/mS typical
Set UVP Debounce	☐
Programmable Voltage Threshold	6 V
Programmable Power Threshold	0 W

(b) To get the 5-V PDO, we can just use the "Port 0 Sink PDO 0 Negotiated" event as this will trigger on the 5V PD contract, but not on the 5-V default.

See the image below for how to configure the GPIO table. If you want to combine these GPIOs into one output, you can configure the I/O with open drain output enable with internal pullups to allow shorting the GPIOs. You can also use them separately.


I/O Config (0x5c)

GPIO #0

Field	Value
Multiplexing for GPIO 0 pin	Pin Multiplexed to GPIO
Initial Value	0x0
Open Drain Output Enable	☑
Internal Pull Down Enable	☐
Internal Pull Up Enable	☑
Mapped Event	Port 0 Sink Greater Than Threshold Event
GPIO Polarity	Direct-mapped Event

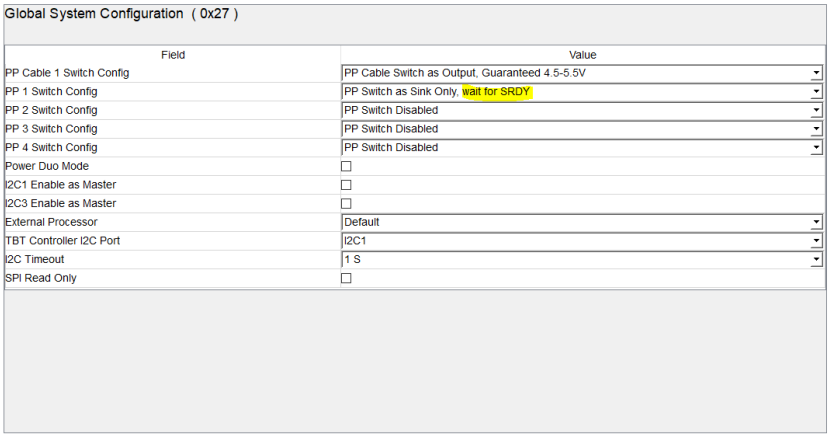
GPIO #1

Field	Value
Multiplexing for GPIO 1 pin	Pin Multiplexed to GPIO
Initial Value	0x0
Open Drain Output Enable	☑
Internal Pull Down Enable	☐
Internal Pull Up Enable	☑
Mapped Event	Port 0 Sink PDO 0 Negotiated
GPIO Polarity	Direct-mapped Event

(2) Next is configuring a GPIO that will enable/disable the power path.

For this, we will go back to the Wait for ‘SRDY’ and ‘SRDY’ functionality mentioned earlier.

The first step is configuring the sink power path to be “Wait for SRDY” which is done in the Global System Configuration register.


Global System Configuration (0x27)

Field	Value
PP Cable 1 Switch Config	PP Cable Switch as Output, Guaranteed 4.5-5.5V
PP 1 Switch Config	PP Switch as Sink Only, wait for SRDY
PP 2 Switch Config	PP Switch Disabled
PP 3 Switch Config	PP Switch Disabled
PP 4 Switch Config	PP Switch Disabled
Power Duo Mode	☐
I2C1 Enable as Master	☐
I2C3 Enable as Master	☐
External Processor	Default
TBT Controller I2C Port	I2C1
I2C Timeout	1 S
SPI Read Only	☐

Next is the GPIO event. There is a GPIO event called “Port 0 Load App Config 1 Event” that acts as an input. When this GPIO is asserted, it will load an “Virtual Device”. This is mainly used to load a slightly different register configuration on top of the current one. Part of loading the device also includes sending a single 4CC command upon entry. We are only interested in the 4CC part, not the register configuration.

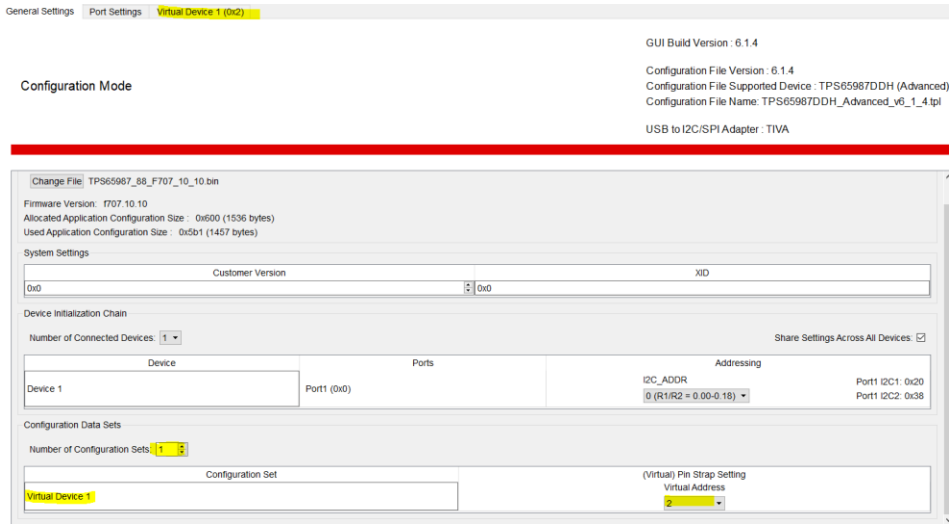
Configuration of this GPIO requires a couple steps.

First set the GPIO to the correct event.

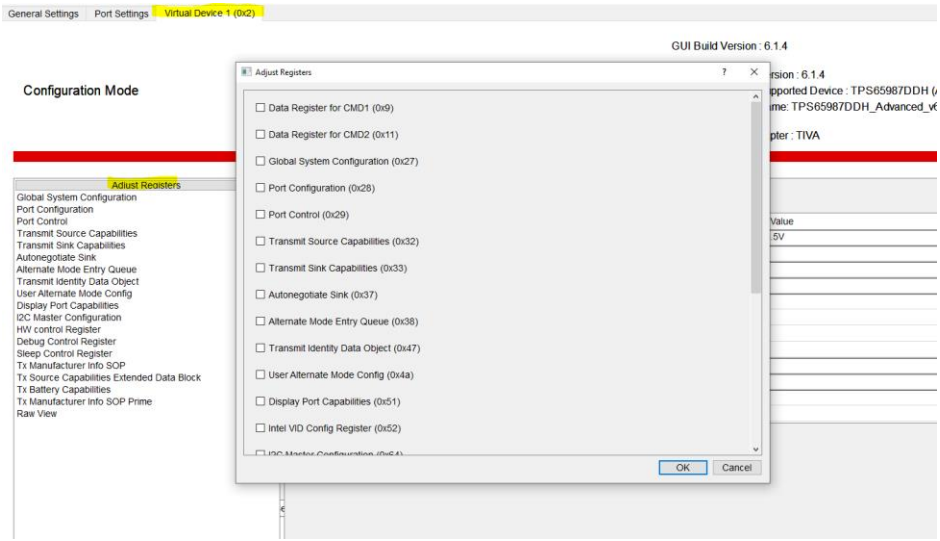
GPIO #2

Field	Value
Multiplexing for GPIO 2 pin	Pin Multiplexed to GPIO
Internal Pull Down Enable	☐
Internal Pull Up Enable	☐
Mapped Event	Port 0 Load App Config 1 Event
GPIO Polarity	Direct-mapped Event

Next, Enable a Virtual device so we can configure the settings. This is done in the General settings tab in the Configuration Data Sets section. Increment the number of configuration sets to 1. This will open a new tab at the top for the new virtual device.

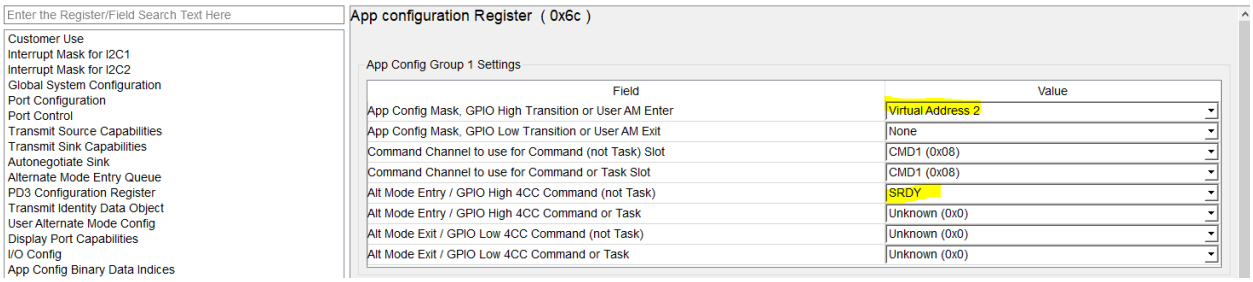


Go to the virtual device and remove all the registers by going to “Adjust Registers” and de-selecting all registers.



Next, got to “Port Settings”, “App Configuration Register”. Because we chose the GPIO event “Port 0 Load App Config 1 Event”, we are interested in APP config Group 1. Set the First field to match the virtual address for the Virtual Device. In this case, it should be 2.

Then configure the 4CC command to send on Alt Mode entry, in this case SRDY.



Now the GPIO and system should be configured.

You should be able to tie the two output GPIOs(1) to this input GPIO(2). What this will do is enable the sink power path for PD contracts, but will not enable it for any default type-C contracts.