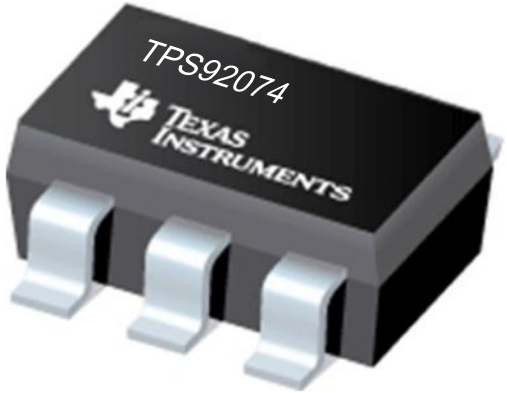
TPS92074/ TPS92075

Non Triac Dimming LED Driver Configurations



Appendix (Slide 25)

TPS92074/075

Non-Isolated, Phase Dimmable, Buck PFC LED Driver with Digital Reference Control

Features

- Application input voltage: 120VAC, 230VAC
- Controlled Reference Derived PFC
- Topology: Non-Isolated Buck or Buck-Boost with PFC
- Constant Current Operation Using Peak Current Mode Control
- Protection Features: VCC Over-Voltage Protection, Cycle-by-Cycle Over-Current Protection, UVLO, Thermal Shutdown
- TSOT6 & SO8 Package Options

Benefits

- Supports All Common Line Voltages
- Meets Regulatory PFC Requirements for LED Lighting
- Compact Design with Low Component Count
- Improved Line and Load Regulation
- Protects Against Fault and Abnormal Operating Conditions

Applications

- 5-30W LED Luminaires/lamps
- LED Ballasts / Troffer (T8/10 replacement)

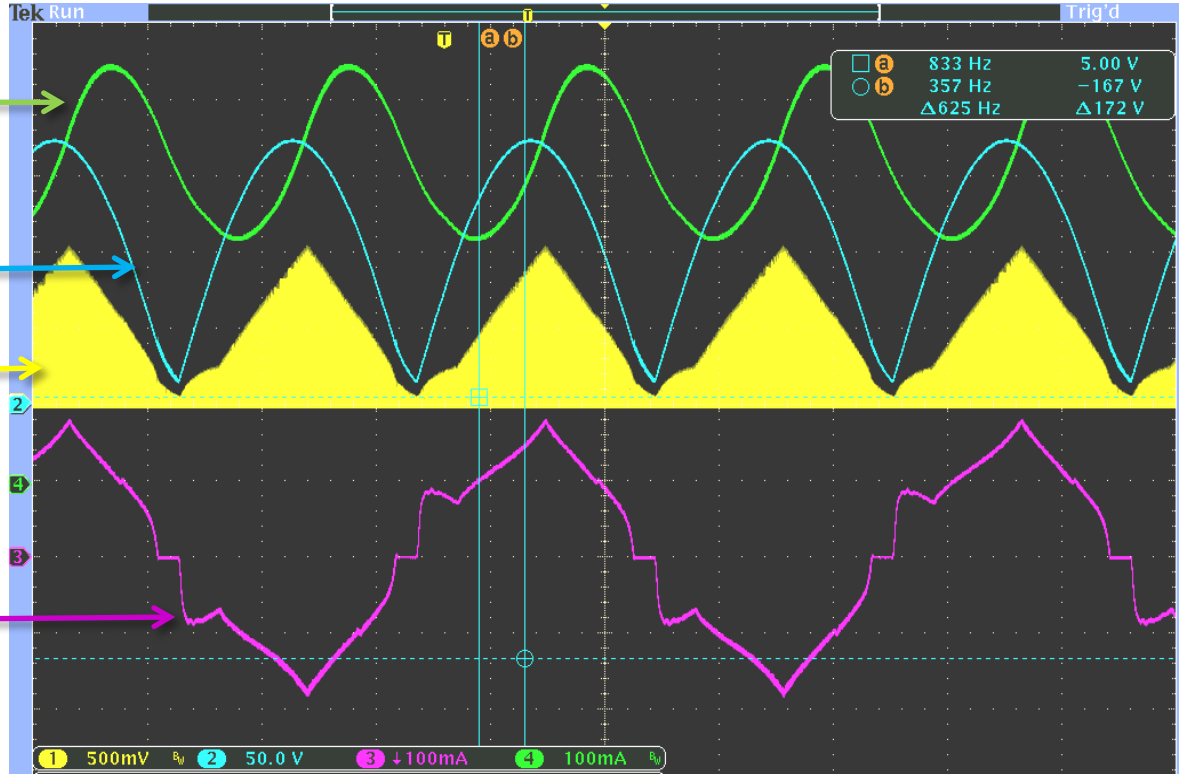
TPS92074 LED Driver – Waveforms in Normal Operation

-LED Current

-Input Voltage

-Current Sense
(following internal DAC)

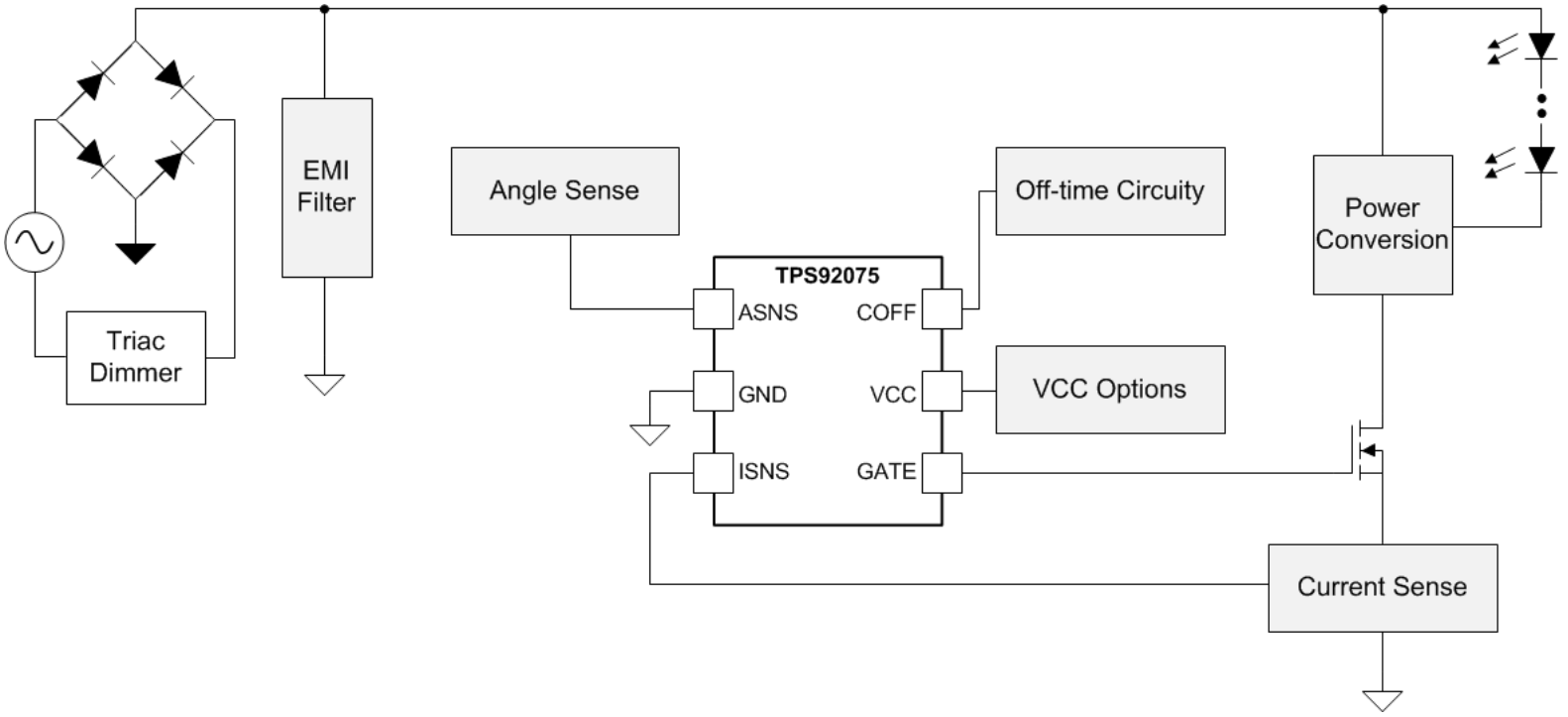
-Input Current



-Non-Dimming Operation: *Output Current Reference Synchronized to the input line voltage*

THD: 17.8 Power Factor: 0.984

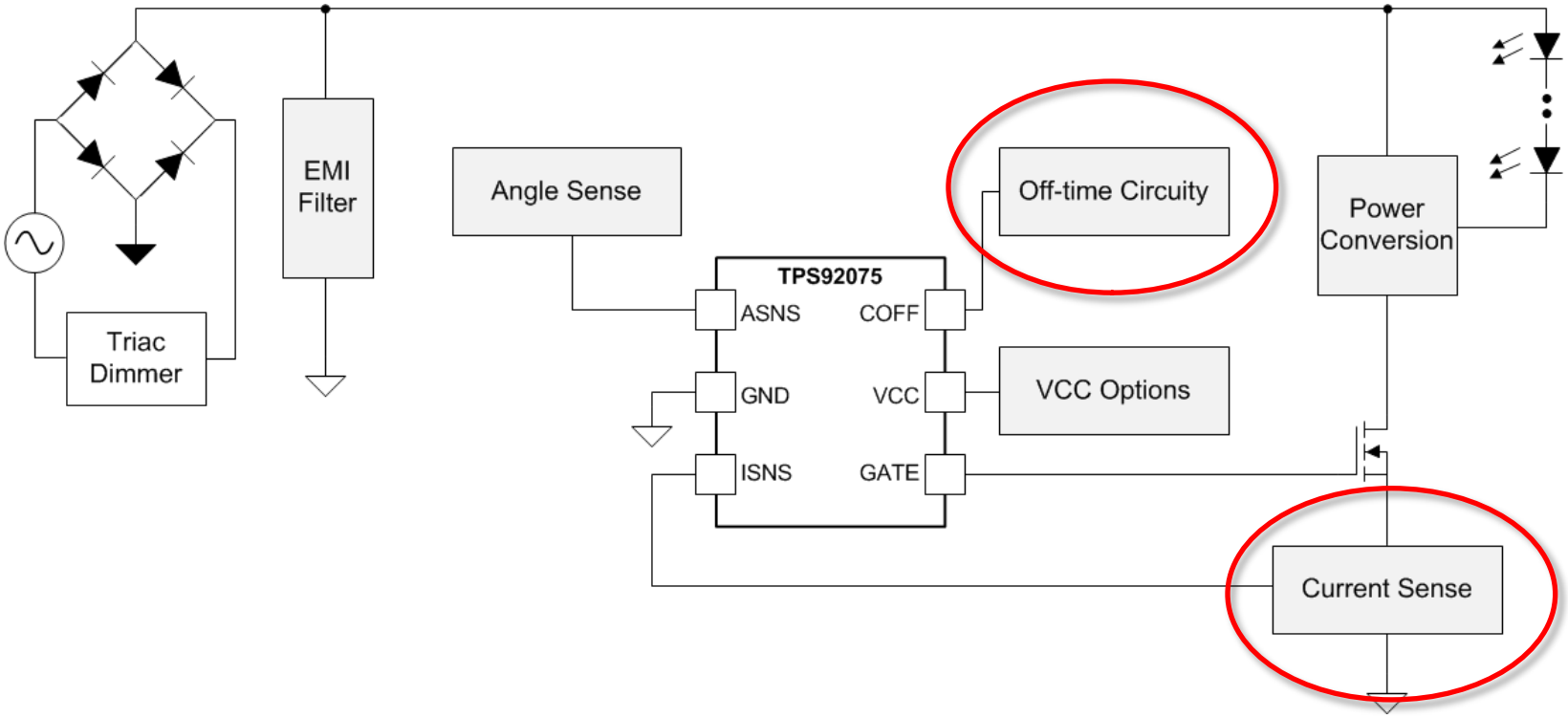
Typical Dimmable LED Driver Main Circuit Blocks



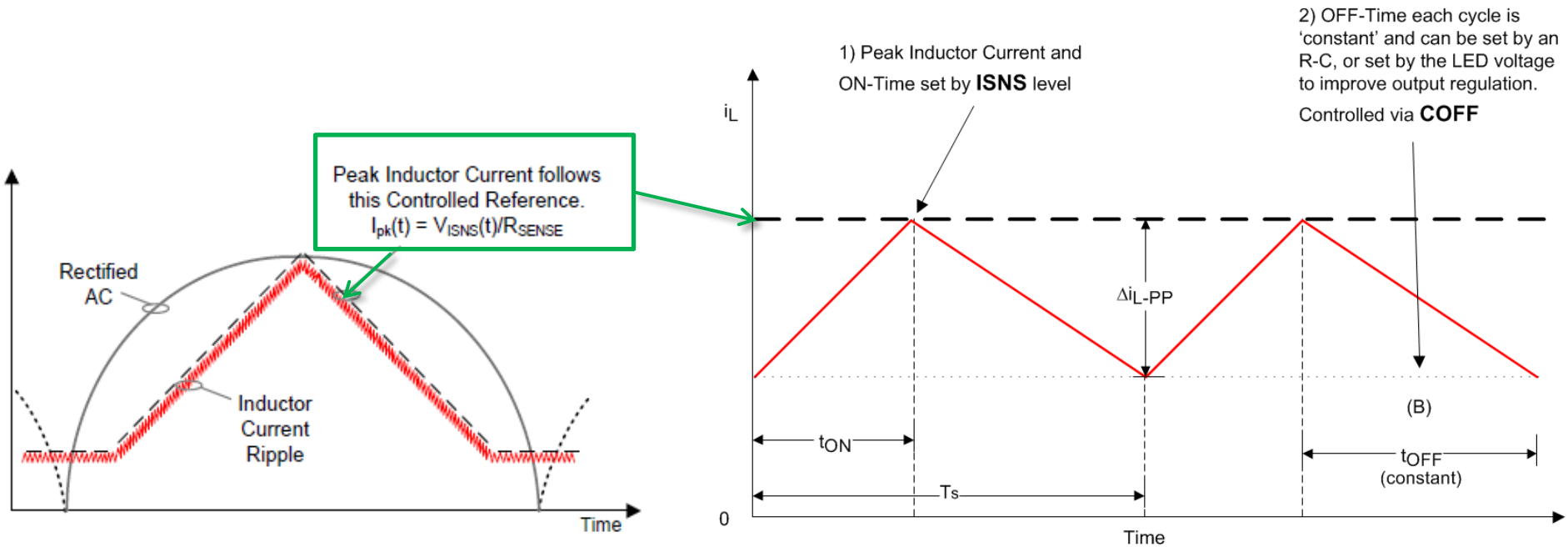
Configuring the TPS92074 is easy!

→Consider a few main circuit blocks

Hysteretic Control



TPS92074 Hysteretic Control



→ASNS Signal → Digital Block and Algorithms → DAC → Comparator

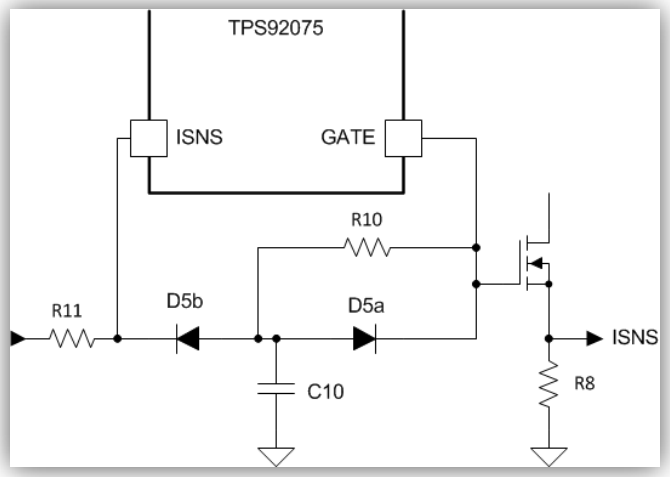
→ Controlled Inductor Peak Current Reference

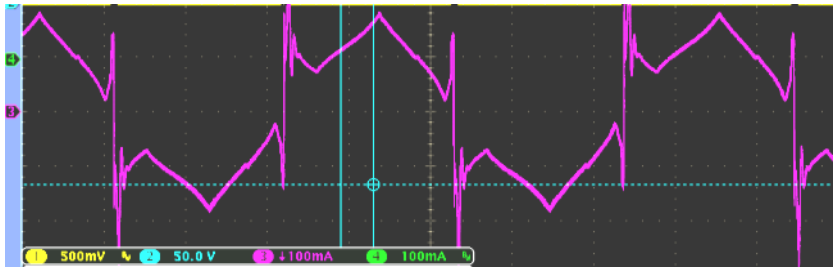
TPS92074 Hysteretic Control – Ton Clamp

Without Ton Clamp:
Current spikes at cycle limits are high

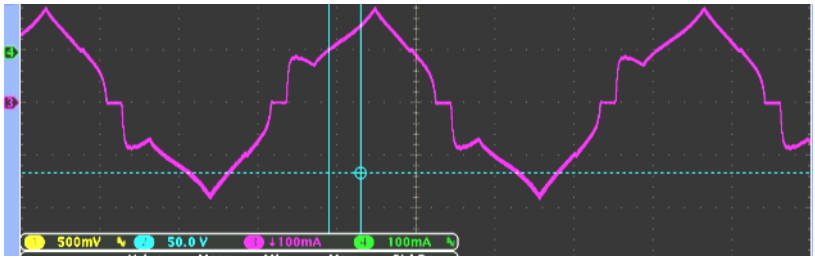
With Ton Clamp
Spikes are eliminated, THD lowered, Triac Compatibility increased

-Ton Clamp components are low cost



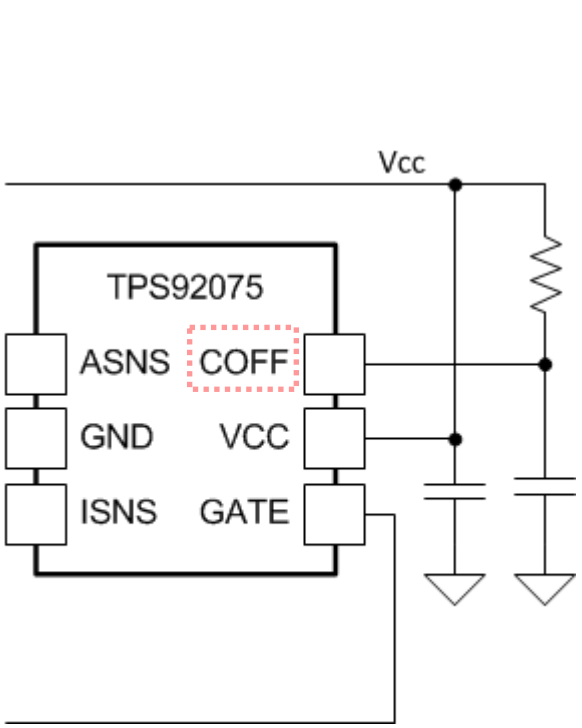


LED Driver Input Current:
Ton Clamp **Not** in Use



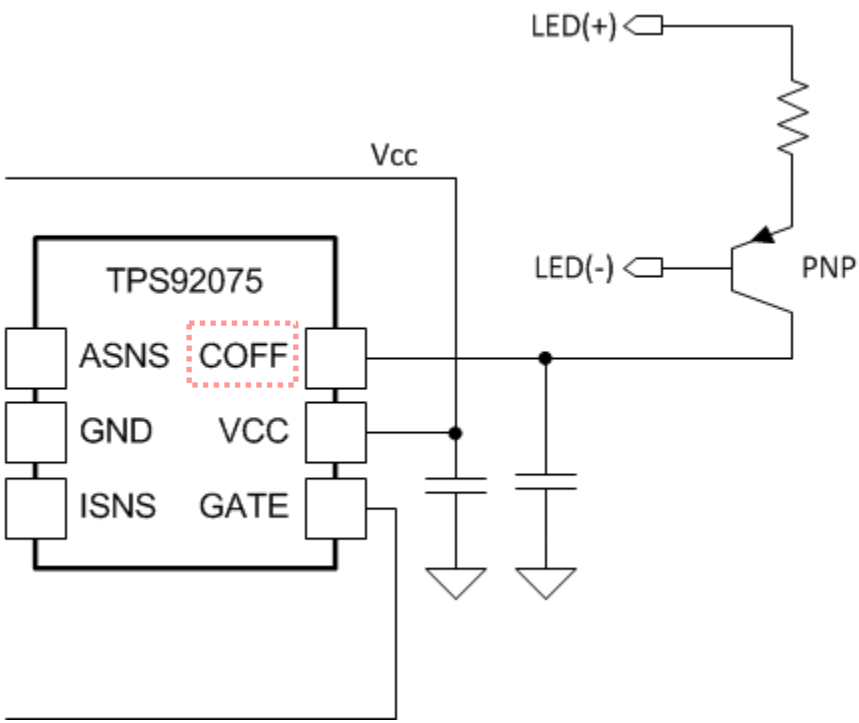
LED Driver Input Current
Ton Clamp **in** Use

TPS92074 Hysteretic Control – Addition of output PNP



←Simple

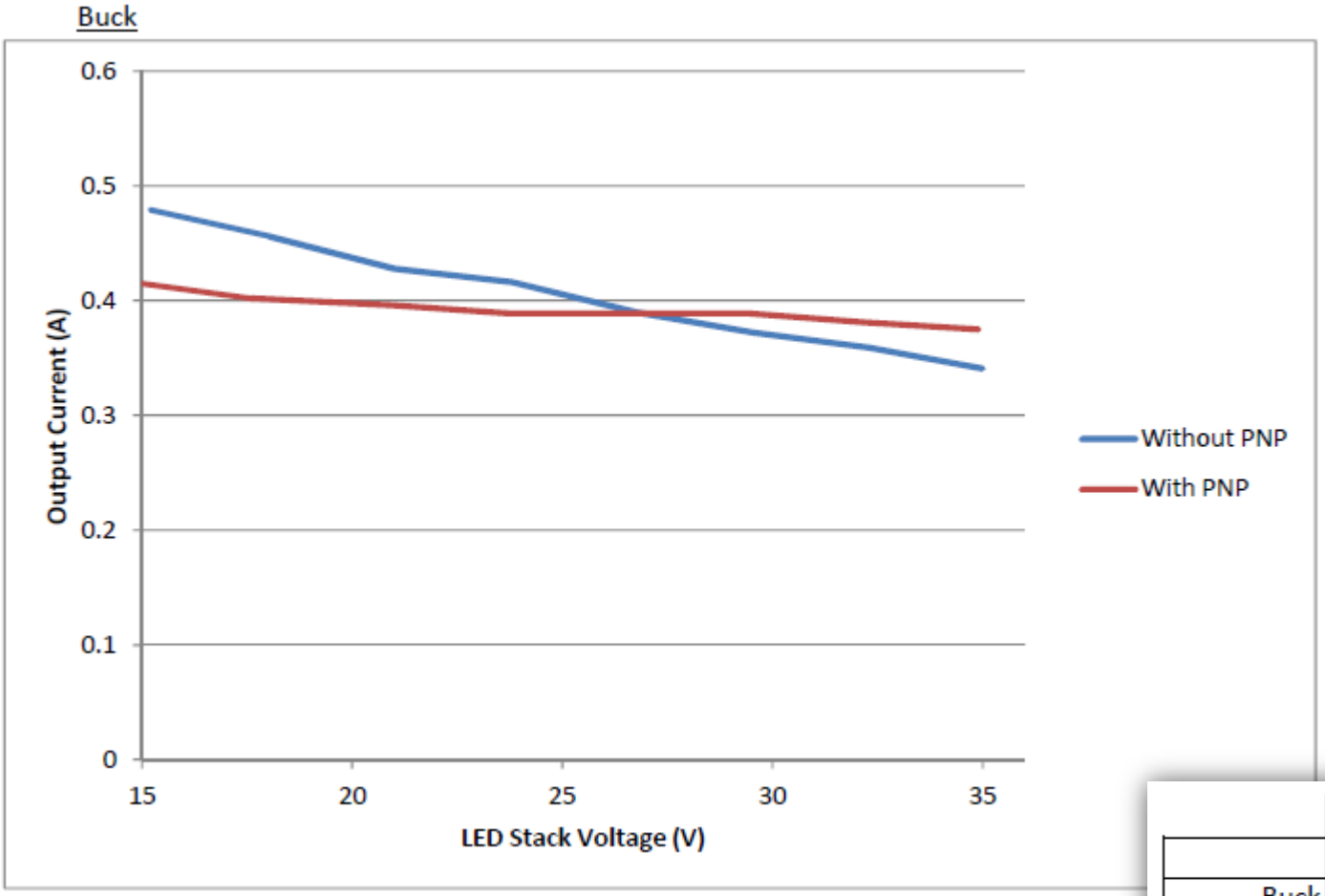
More Accurate→



-Simple circuit addition improves load regulation

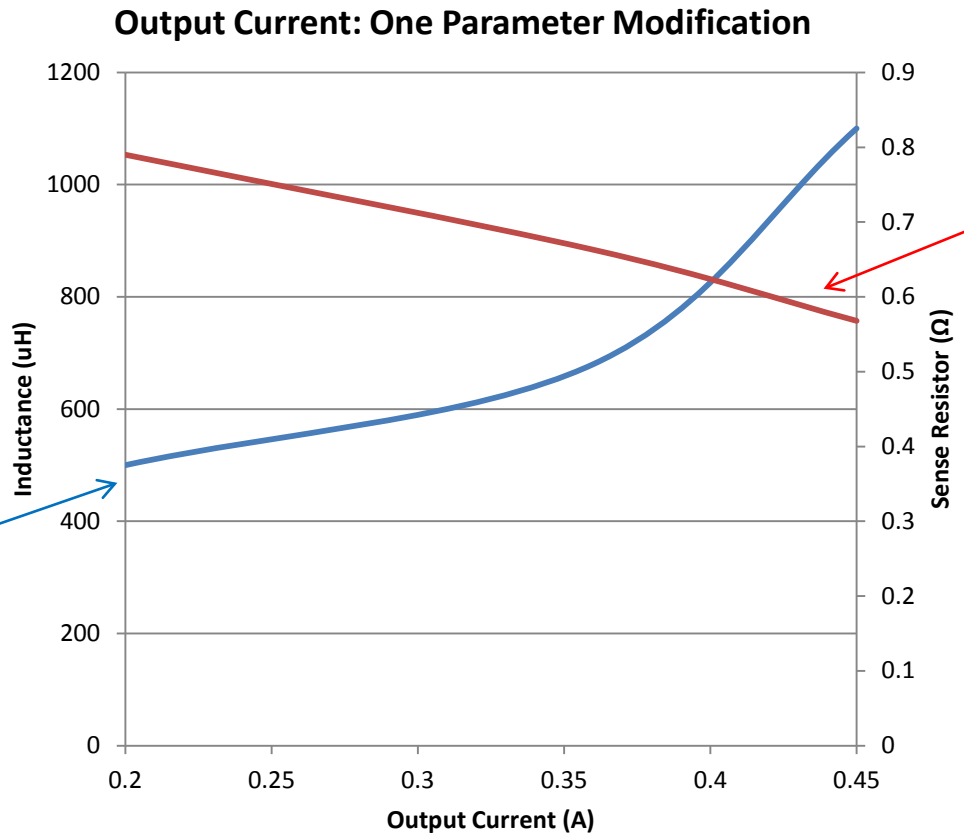
-Off-time can be generated using LED stack voltage

TPS92074 Hysteretic Control – Addition of output PNP



	mA/V change	
	w/o PNP	with PNP
Buck	7	2
Buck Boost	5.6	2.6

Hysteretic Control – Trend of Component Adjustment

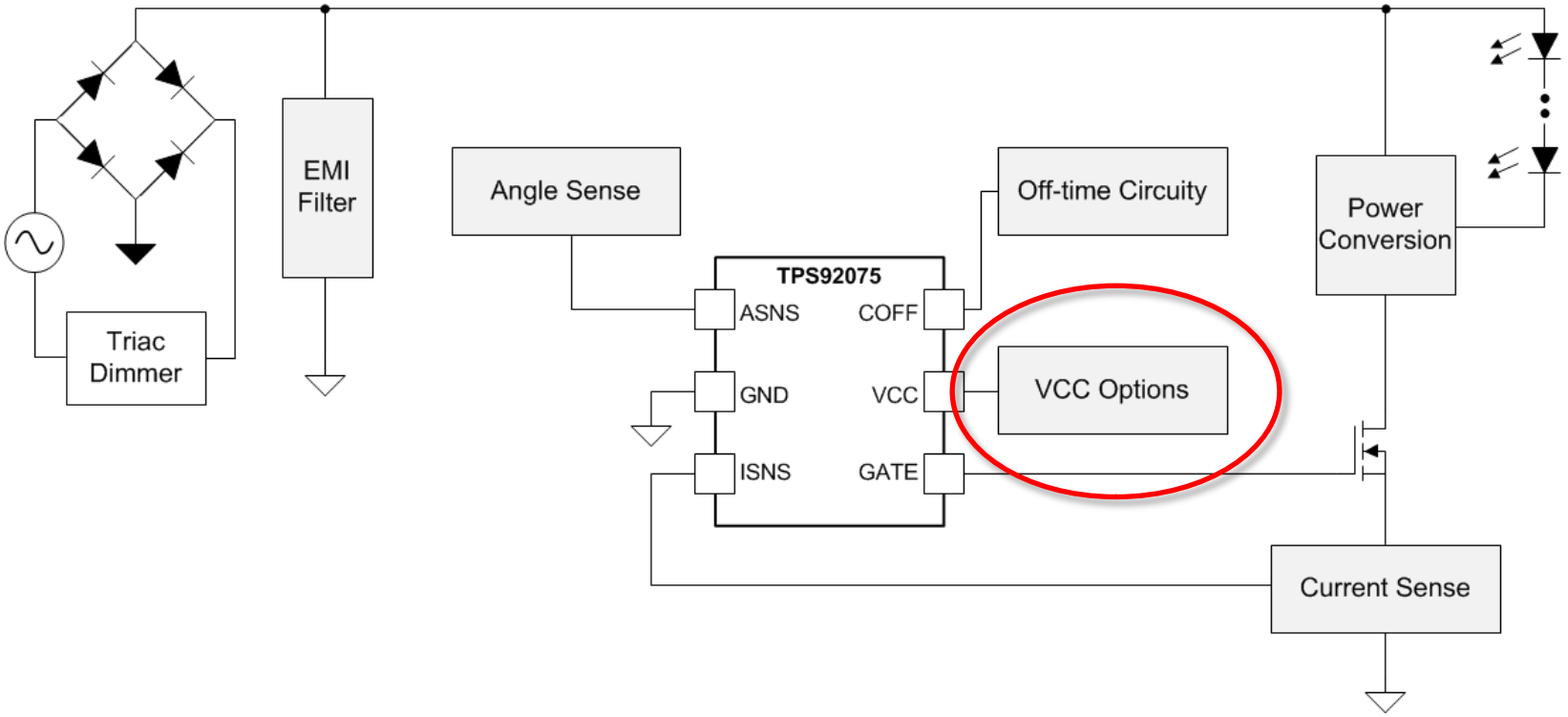


Fix Inductance, Change Sense Resistor

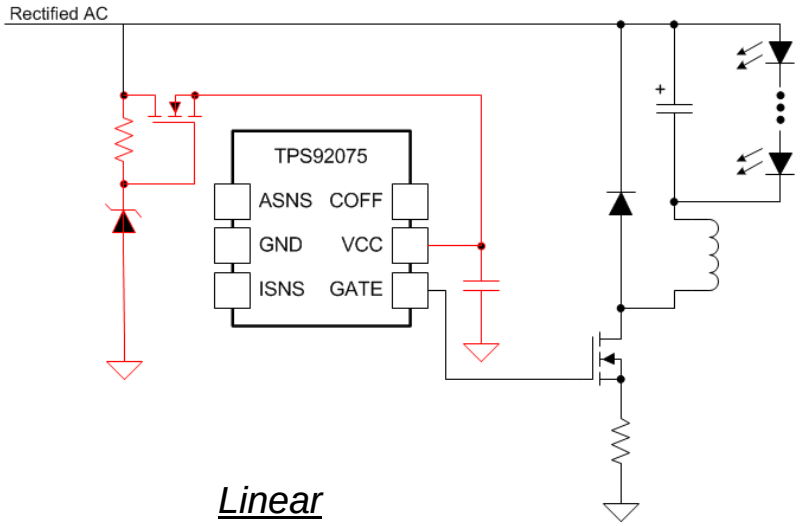
Fix Sense Resistor, Change Inductance

General trend if performed using buck-boost design similar to EVM

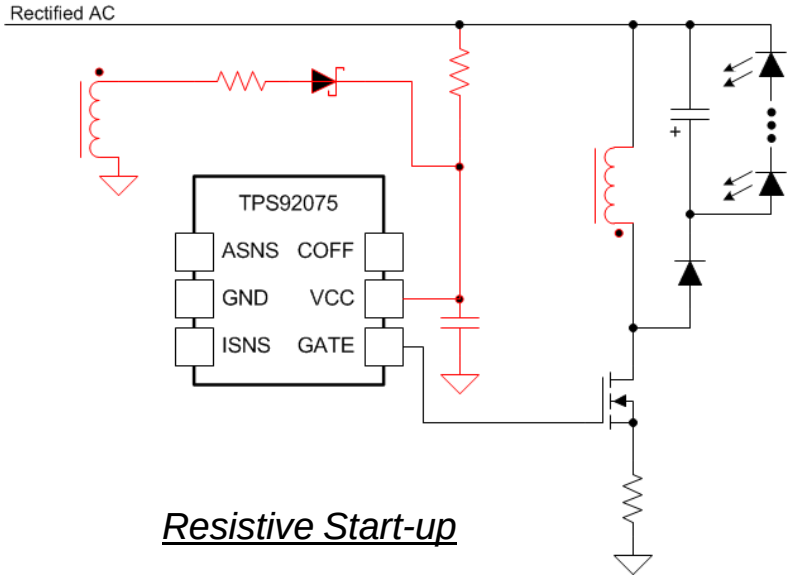
VCC Information and Control



TPS92074 – VCC Options



Linear



Resistive Start-up

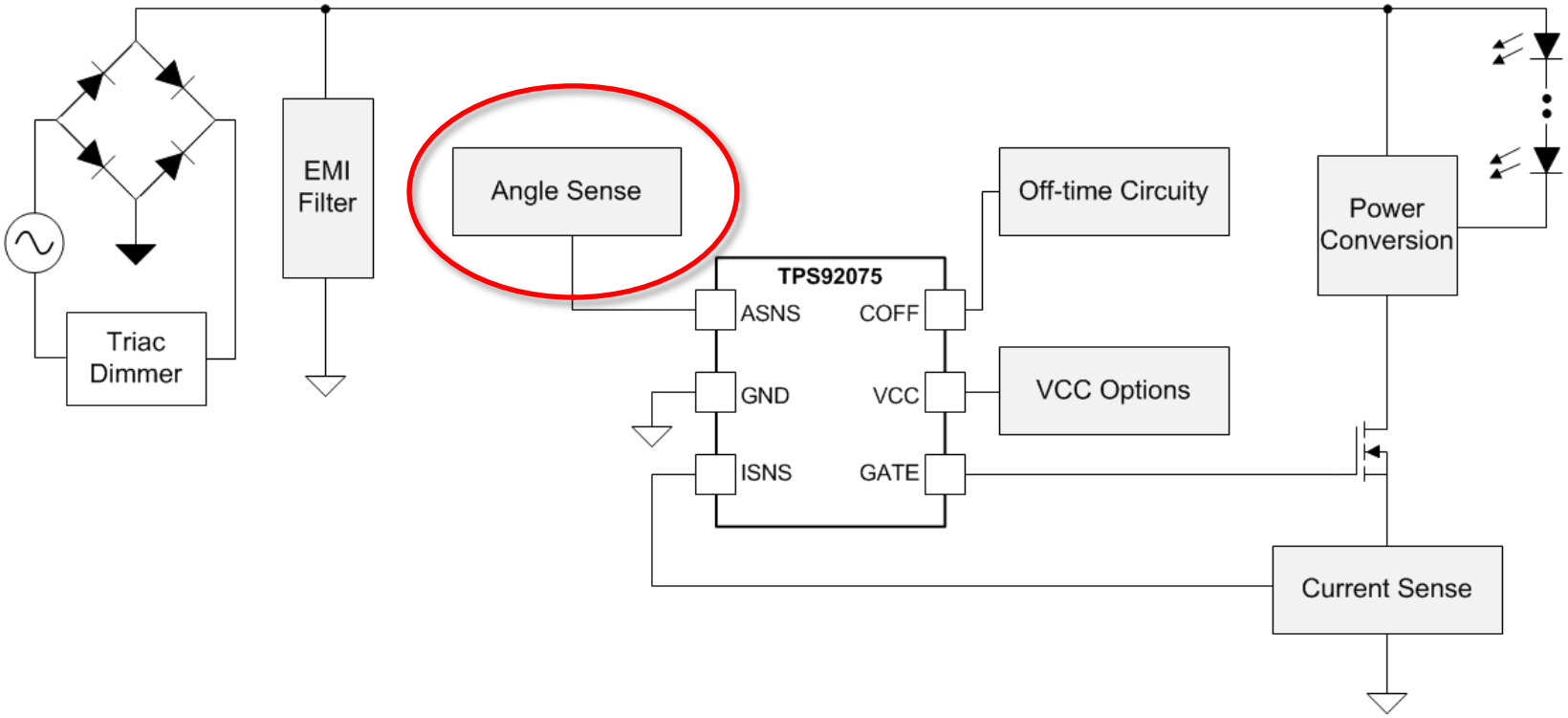
-Basic linear regulator provides the fastest start-up time and if VLED > 20V, no series diode or large VCC capacitor is required

-VCC can be provided from bottom of LED stack for some designs to increase efficiency

-Design considerations have been made to support resistive start-up methods.

-Using AUX provides OVP

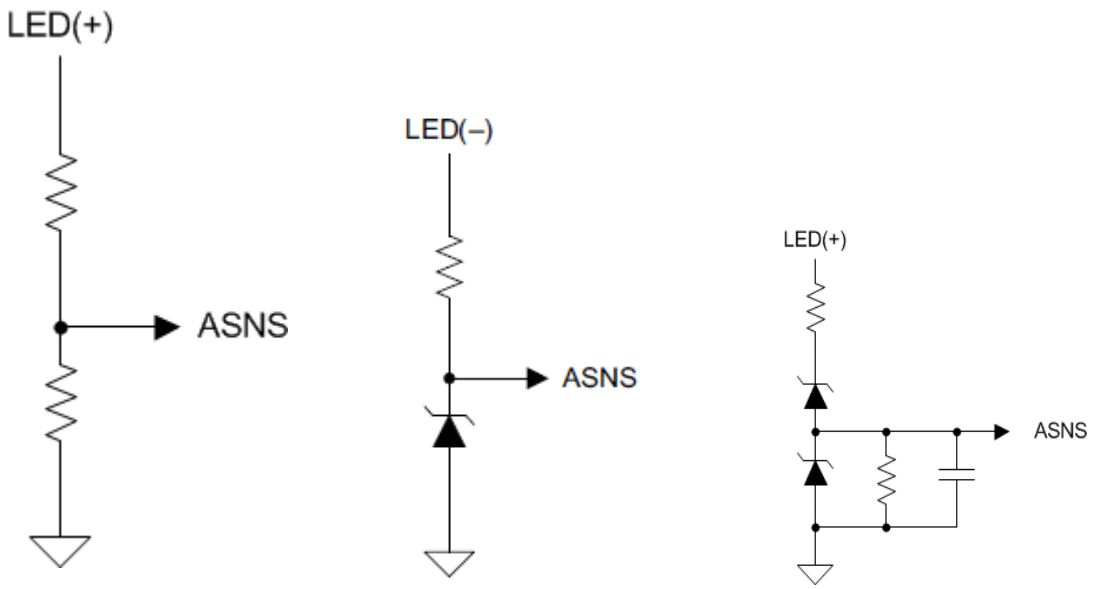
Angle Sense


EMI Filter
Angle Sense
Triac Dimmer
TPS92075
ASNS
COFF
GND
VCC
ISNS
GATE
Off-time Circuity
VCC Options
Power Conversion
Current Sense

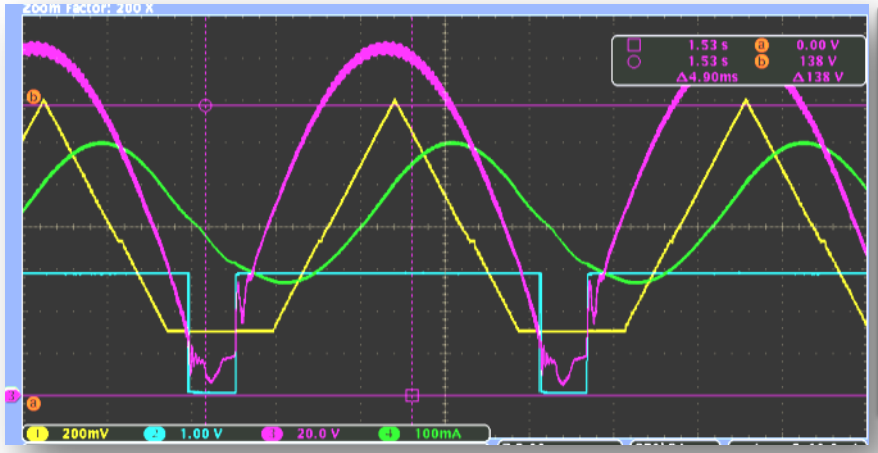
TPS92074 Angle Sense Input

- Options to ensure minimal components used in Buck or Buck-Boost

Need to ensure:
- >70% duty cycle for creation of ramp
- Signal crosses 1V (rising) and 0.5V (falling) when dimming and non-dimming



TPS92074: Phase Locked Ramp



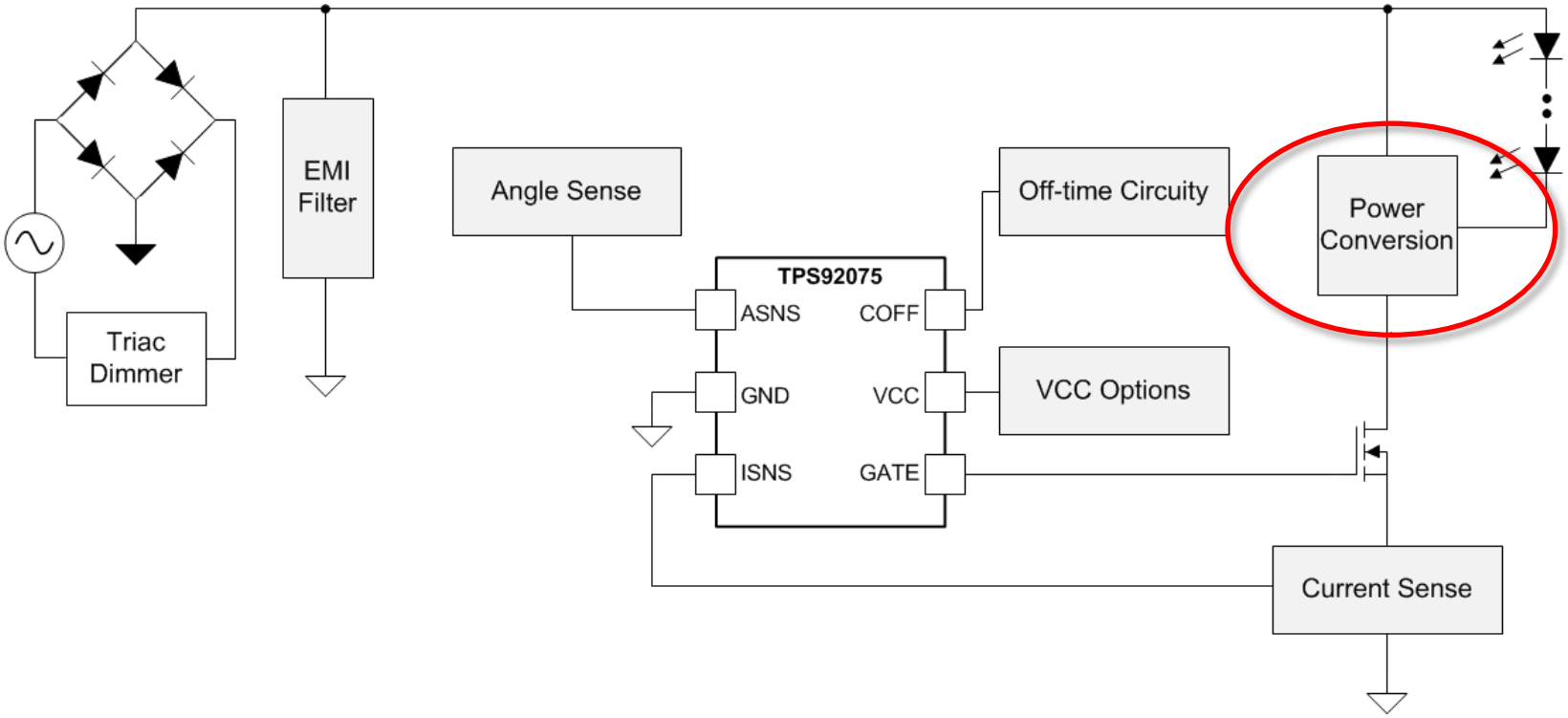
1MHz Clock
+/-25%

÷ clk divide term

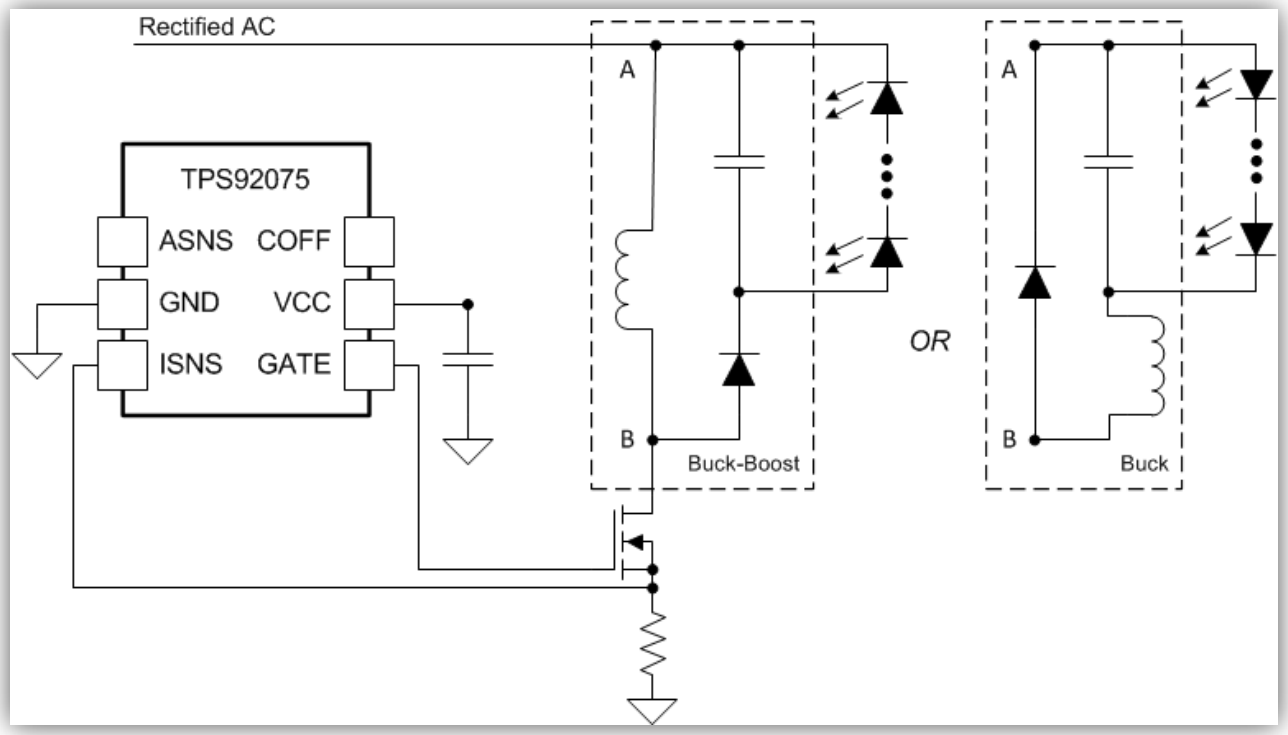
$$\frac{\text{Previous clk divide term} * \text{average of clk divide terms}}{256}$$

Slow Clock
@256 cycles per
line cycle

Power Conversion

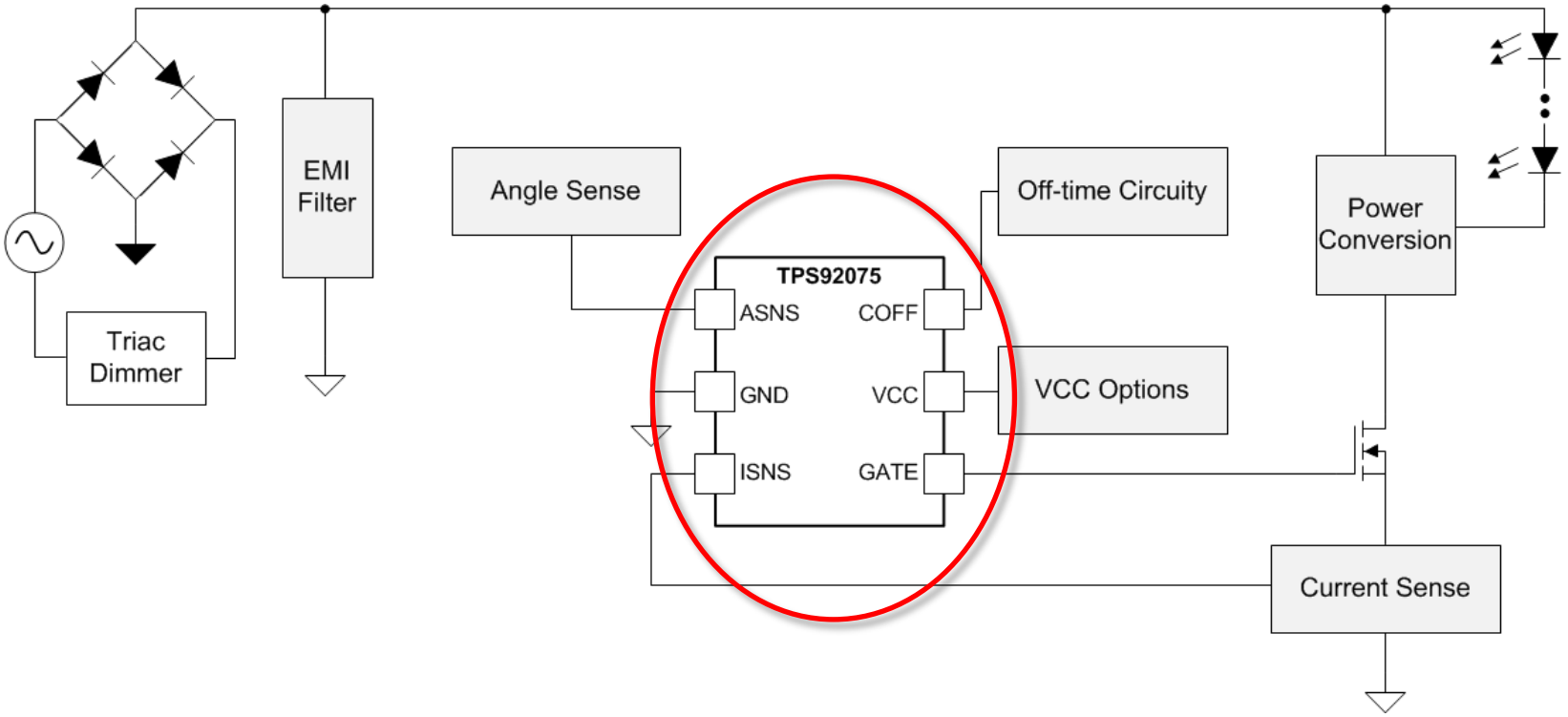


TPS92074 – Power Conversion



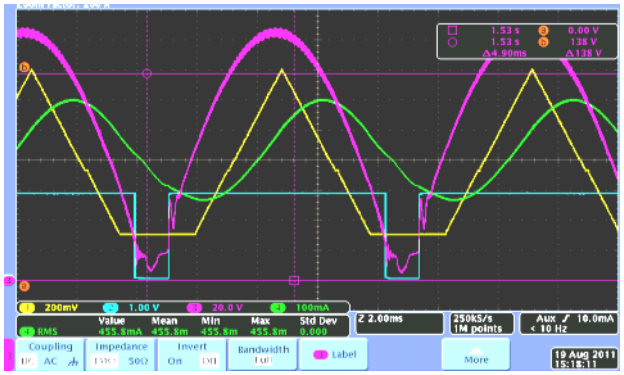
Buck (w/DC Side Filter)		**Buck - Boost**
Wider Dimming Range	↔	Less chance for flicker
Higher Efficiency	↔	More load during dimming
	✔	Only option if <20% THD is required with certain LEDs

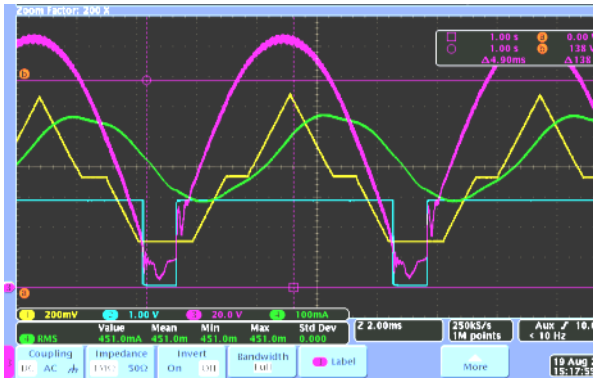
Part Intelligence Features

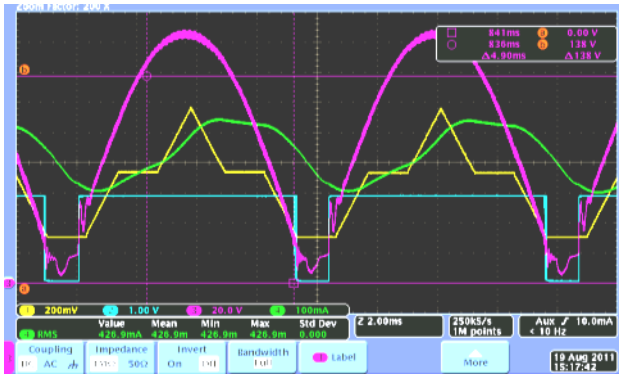


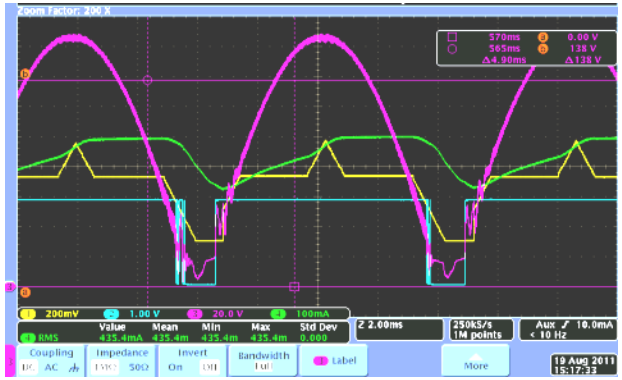
TPS92074 – Morphing to High Power Factor Mode

CH1: Output Current Set Point CH2:Angle Sense **Ch3: Rectified AC** **CH4: LED Current**



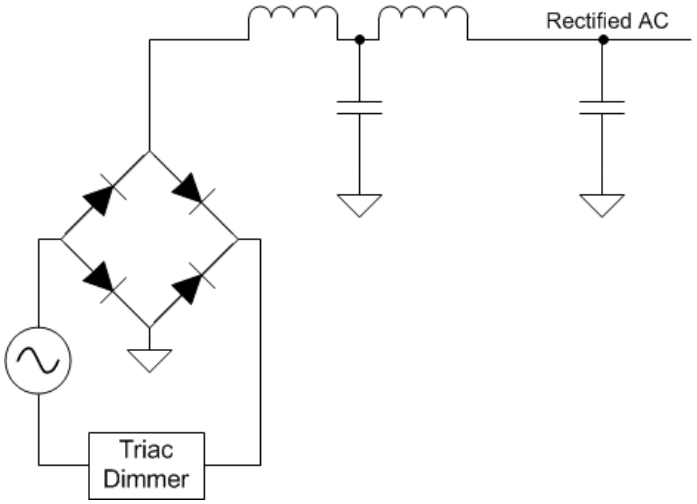


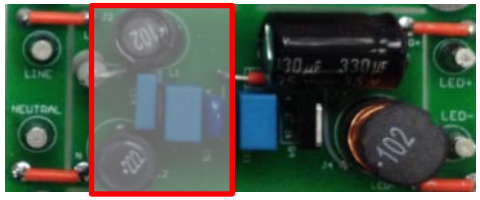




- Internal triangular reference voltage
  - PFC > 0.9
  - Robust operation
- Reference morphing operation
  - Triangular to DC
  - Improved TRIAC dimmer compatibility

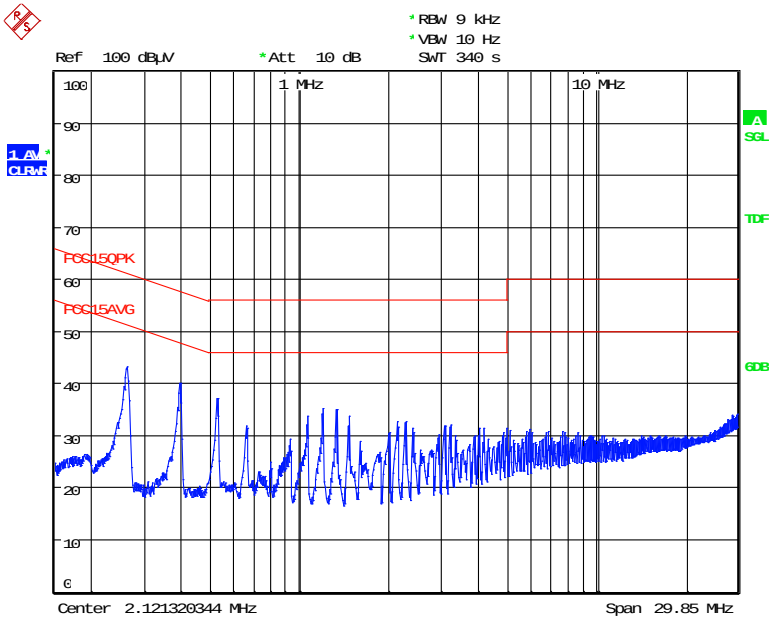
TPS92074 – EMI Filter



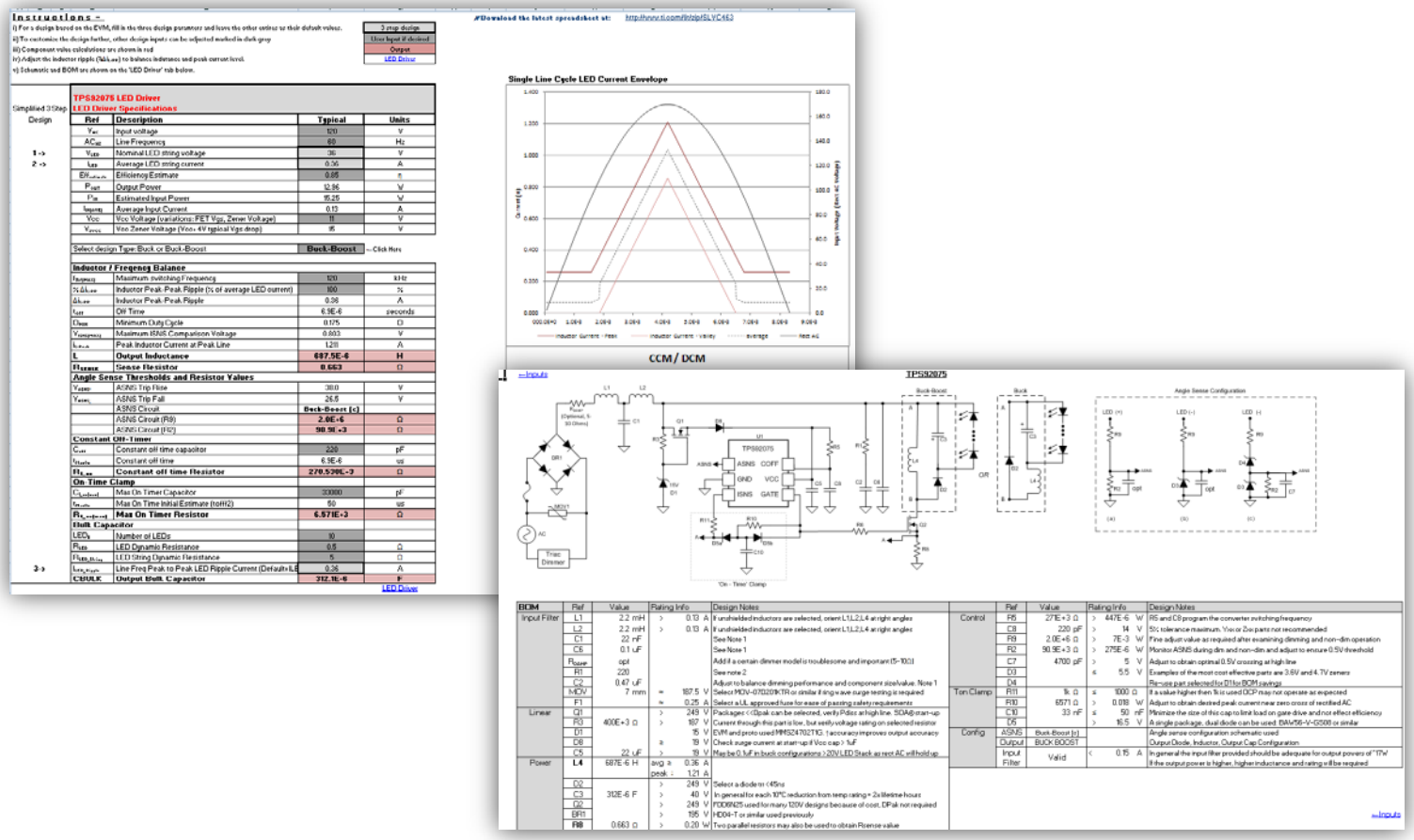


-A simple EMI filter can mitigate conducted EMI.

- Proven filter pole and triac damping configurations



Design Problem using Excel Spreadsheet



Design Problem using Excel Spreadsheet – Buck Option

The design tool also supports BUCK designs

For 120Hz **BUCK** EVM designs, enter:

1) **String Voltage**
2) **LED Current**
3) **Select Topology**
4) **Desired 120Hz LED Current Ripple**

Simplified 3 Step Design

TPS92075 LED Driver
LED Driver Specifications

	Ref	Description	Typical	Units
	V_{AC}	Input voltage	120	V
	AC_{HZ}	Line Frequency	60	Hz
1 ->	V_{LED}	Nominal LED string voltage	36	V
2 ->	I_{LED}	Average LED string current	0.36	A
	$Eff_{estimate}$	Efficiency Estimate	0.85	η
	P_{OUT}	Output Power	12.96	W
	P_{IN}	Estimated Input Power	15.25	W
	$I_{IN(AVE)}$	Average Input Current	0.13	A
	Vcc	Vcc Voltage (variations: FET Vgs, Zener Voltage)	11	V
	V_{ZVCC}	Vcc Zener Voltage (Vcc+ 4V typical Vgs drop)	15	V

Select design Type: Buck or Buck-Boost — **Buck-Boost** (Buck / Buck-Boost)

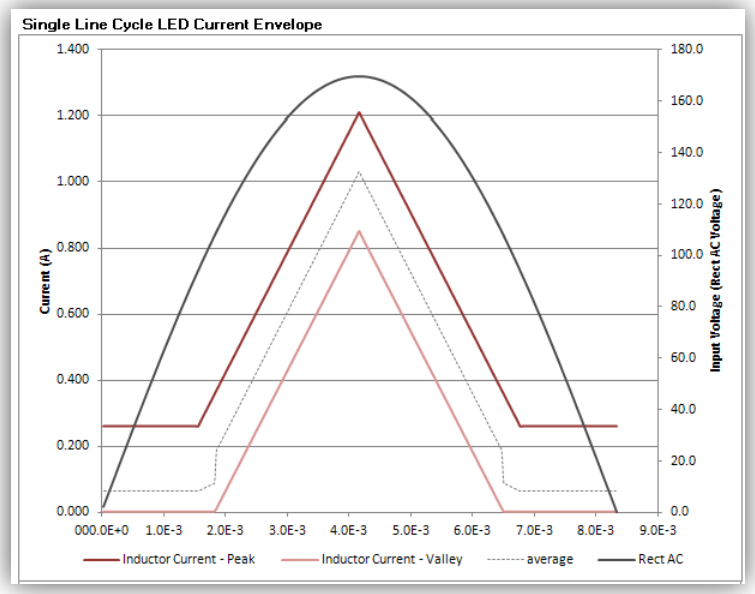
	Bulk Capacitor			
	$LED_\#$	Number of LEDs	10	
	R_{LED}	LED Dynamic Resistance	0.5	Ω
	R_{LED_String}	LED String Dynamic Resistance	5	Ω
3->	I_{LED_Ripple}	Line Freq Peak to Peak LED Ripple Current (Default=ILE	0.36	A
	CBULK	**Output Bulk Capacitor**	**312.1E-6**	**F**

TPS92074 Excel Spreadsheet: Magnetic Optimization

Inductor / Freqency Balance			
$f_{SW(MAX)}$	Maximum switching Frequency	120	kHz
% Δi_{L-PP}	Inductor Peak-Peak Ripple (% of average LED current)	100	%

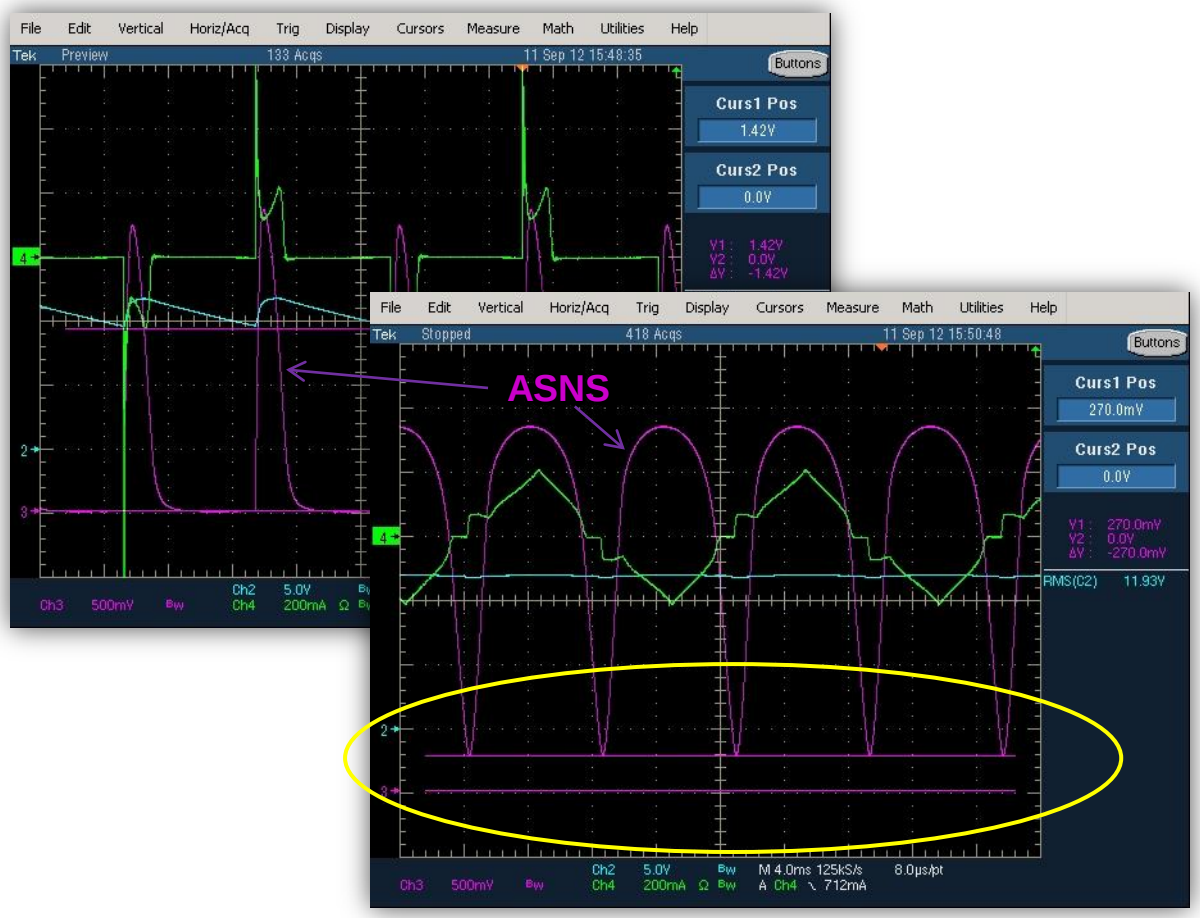
-To fine-tune your design adjust switching frequency and Inductor Peak-Peak Ripple

- Visualize your results over a line cycle



TPS92074 Excel Spreadsheet: Check Final Design ASNS Signal

Upon powering up a new design, check the ASNS signal first!

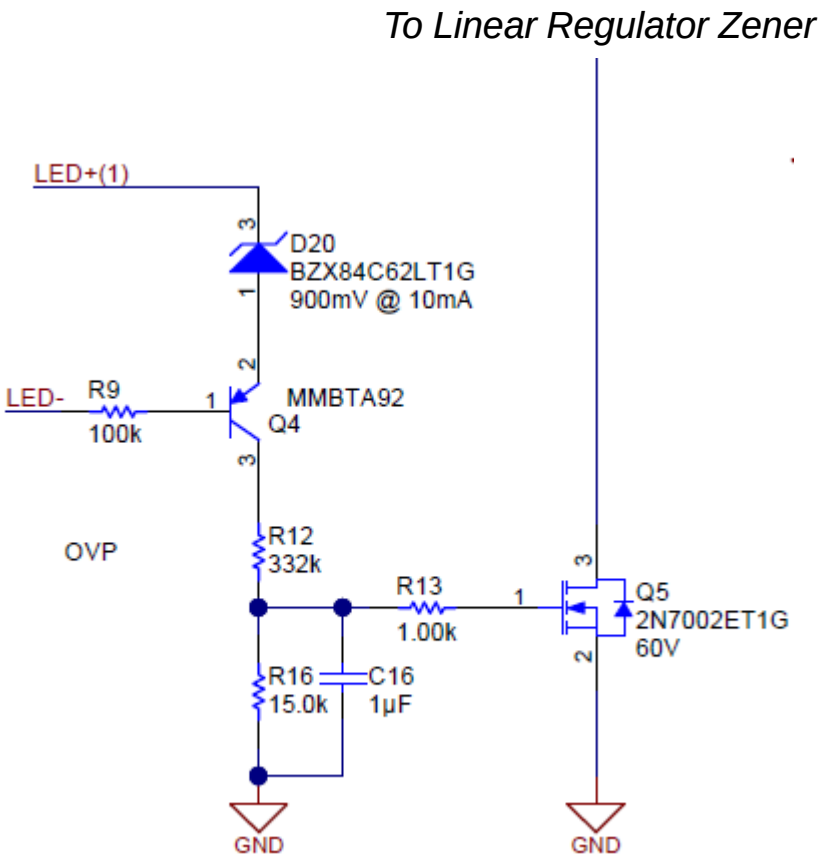


Verify ASNS Signal:

a) Crosses 1V Rising
b) Crosses 0.5V Falling
c) Duration between these levels is >70% duty cycle to engage ramp creation

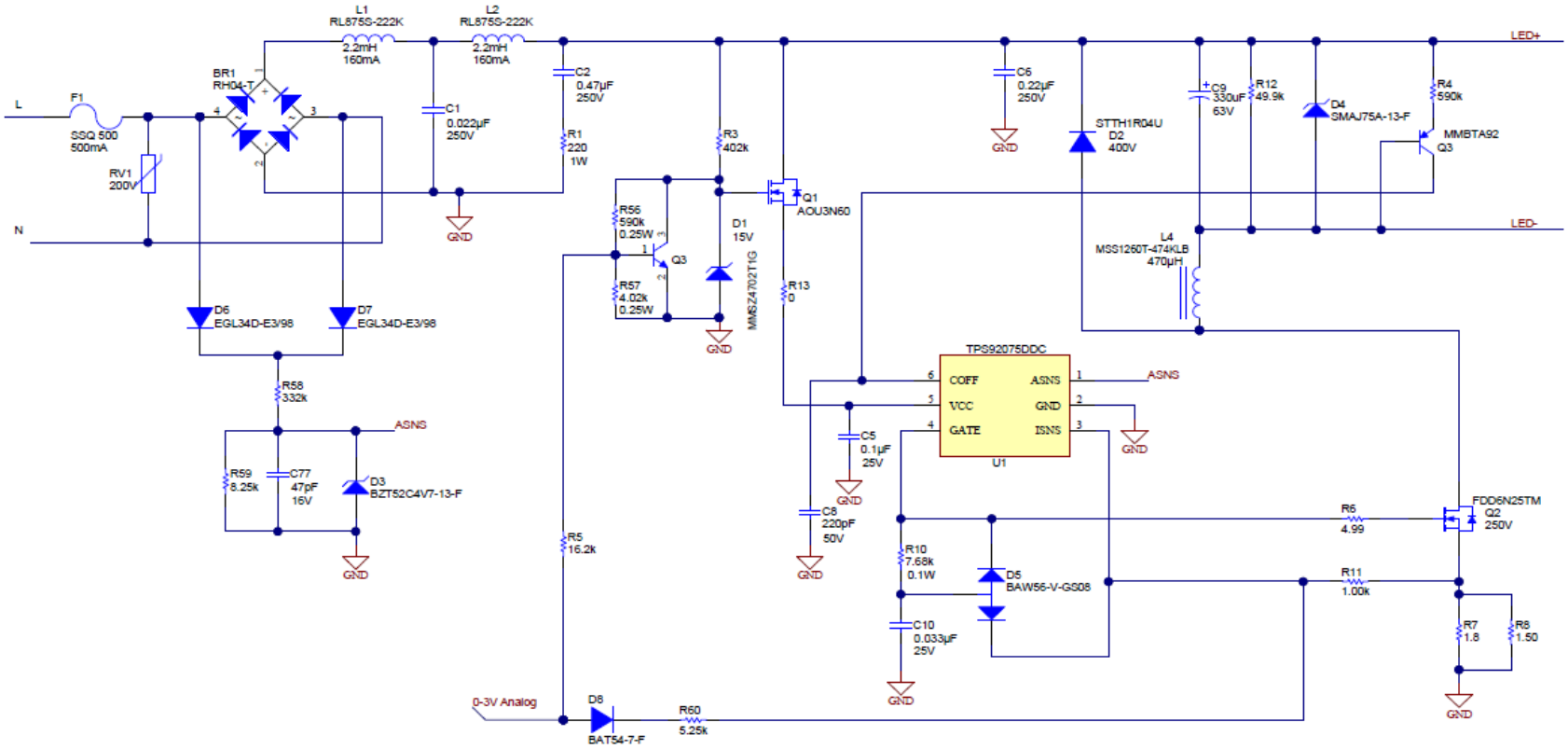
APPENDIX

APPENDIX – *OVP (Over Voltage Protection)*



APPENDIX – (1) *Analog Dimming to Output OFF*

TPS92075 Analog Dimming to OFF with low THD - Preliminary Results



Vcontrol	Iout %	Iout	Vout	PF	THD	Pout	Pin	Efficiency
0.00	100	0.326	39.50	0.985	16.400	12.88	14.54	88.6
0.80	98	0.318	39.12	0.981	19.900	12.44	14.18	87.7
2.00	42	0.136	36.45	0.854	61.000	4.96	5.90	84.0
3.00	8	0.027	33.62	0.754	82.000	0.91	1.48	61.3

D8 used was EGL34D-E3, this will affect output current curve.

APPENDIX – (2) *Analog Dimming to a Minimum (not to OFF)*

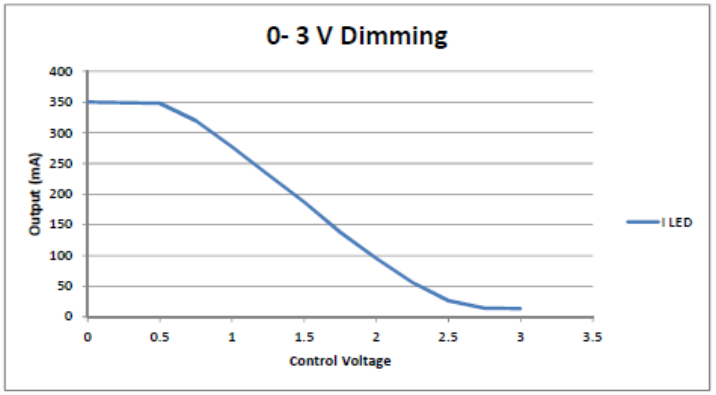
TPS92075 Analog Dimming, initial testing. Buck Boost Implementation

Circuit 1, No ASNS with Ton Clamp

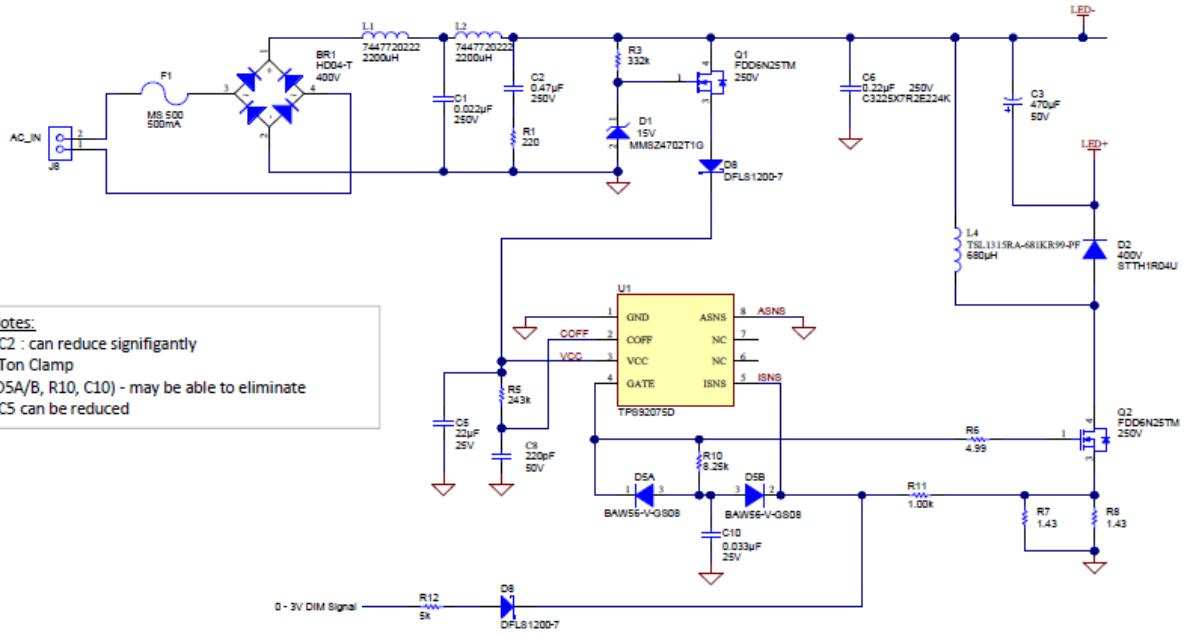
10 LEDs

Vcontrol	I LED
0	350
0.5	348
0.75	320
1	277
1.25	232
1.5	187
1.75	138
2	95
2.25	56
2.5	26
2.75	14
3	13

Non-Dim PF: 0.72



Schematic Tested, No ASNS Used



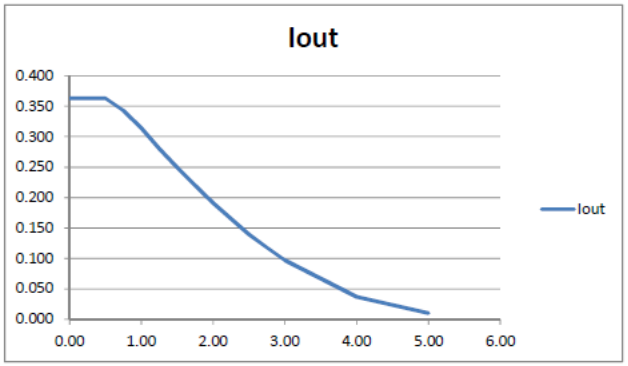
Notes:
- C2 : can reduce signifigantly
- Ton Clamp
(D5A/B, R10, C10) - may be able to eliminate
- C5 can be reduced

APPENDIX – (3) *Analog Dimming to a Minimum (not to OFF)*

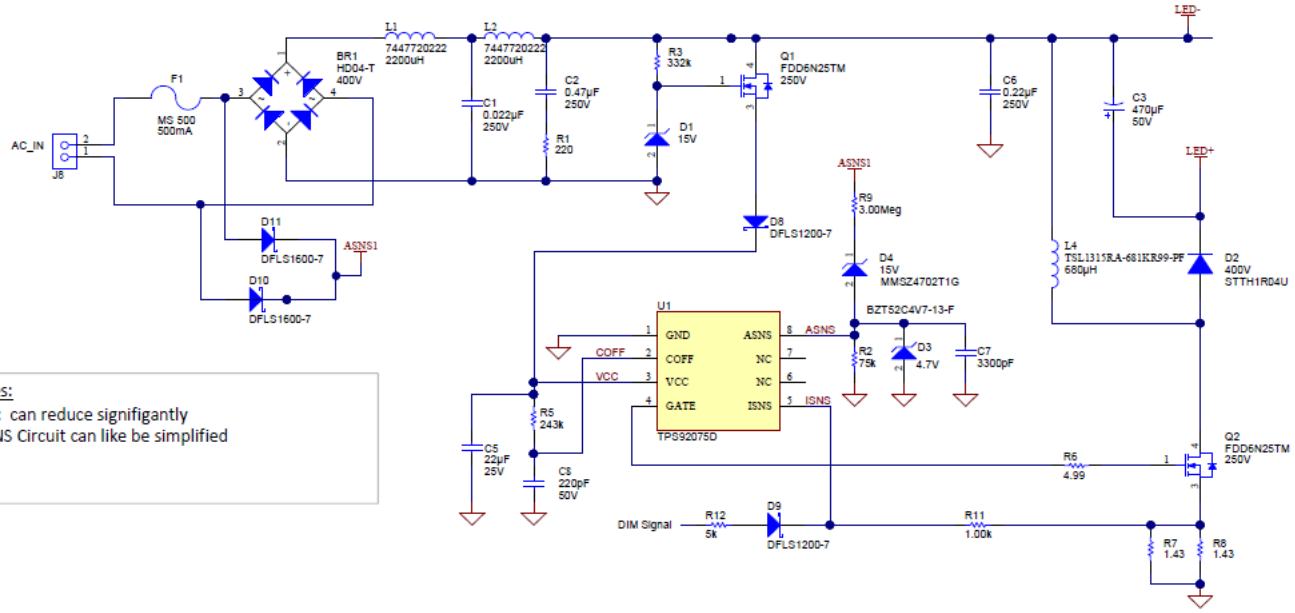
Circuit 2 - ASNS in use, no Ton clamp

ASNS in use, R12 = 2k or 5k Ohms

Vcontrol R12 = 2k	Vcontrol R12 = 5k	Iout	PF	THD	Vout	Pout	Pin	n
0.00	0.00	0.363	0.945	29	35.30	12.82	14.9	0.860
0.50	0.50	0.363	0.945	29	35.30	12.81	14.9	0.860
	0.75	0.343	0.967	23	34.60	11.87	13.98	0.849
	1.00	0.314	0.957	28	34.38	10.80	12.73	0.848
	1.25	0.280	0.938	36	34.16	9.56	11.34	0.843
	1.50	0.250	0.922	42	33.97	8.49	10.05	0.845
↓	1.75	0.220	0.906	46	33.80	7.44	8.85	0.840
	2.00	0.191	0.890	52	33.63	6.42	7.75	0.829
	2.25	0.165	0.870	56	33.47	5.52	6.7	0.824
	2.50	0.140	0.852	61	33.30	4.66	5.77	0.808
	2.75	0.118	0.833	66	33.10	3.91	4.9	0.797
	3.00	0.097	0.818	71	33.00	3.20	4.1	0.781
	4.00	0.037	0.772	80	32.00	1.18	1.88	0.630
3.00	5.00	0.010	0.710	86	31.08	0.31	0.96	0.324



Schematic Tested, ASNS in Use



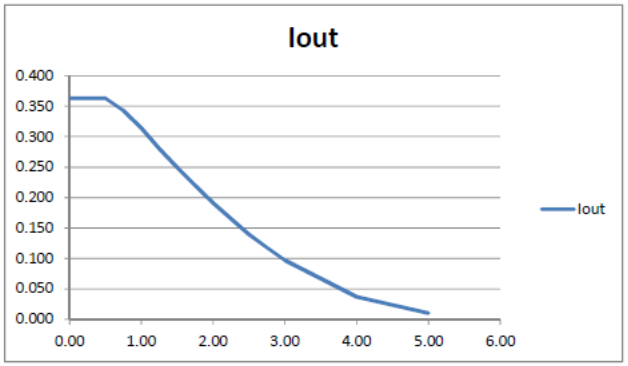
Notes:
- C2 : can reduce signifigantly
- ASNS Circuit can like be simplified

APPENDIX – (3) *Analog Dimming to a Minimum (not to OFF)*

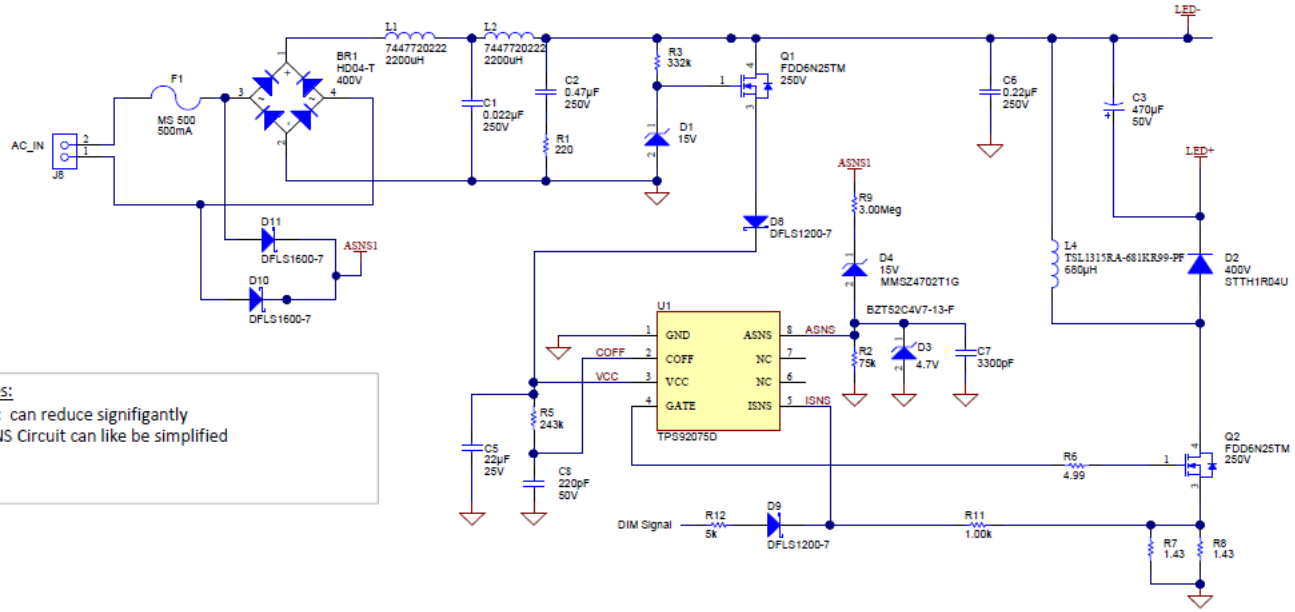
Circuit 2 - ASNS in use, no Ton clamp

ASNS in use, R12 = 2k or 5k Ohms

Vcontrol R12 = 2k	Vcontrol R12 = 5k	Iout	PF	THD	Vout	Pout	Pin	n
0.00	0.00	0.363	0.945	29	35.30	12.82	14.9	0.860
0.50	0.50	0.363	0.945	29	35.30	12.81	14.9	0.860
	0.75	0.343	0.967	23	34.60	11.87	13.98	0.849
	1.00	0.314	0.957	28	34.38	10.80	12.73	0.848
	1.25	0.280	0.938	36	34.16	9.56	11.34	0.843
	1.50	0.250	0.922	42	33.97	8.49	10.05	0.845
↓	1.75	0.220	0.906	46	33.80	7.44	8.85	0.840
	2.00	0.191	0.890	52	33.63	6.42	7.75	0.829
	2.25	0.165	0.870	56	33.47	5.52	6.7	0.824
	2.50	0.140	0.852	61	33.30	4.66	5.77	0.808
	2.75	0.118	0.833	66	33.10	3.91	4.9	0.797
	3.00	0.097	0.818	71	33.00	3.20	4.1	0.781
	4.00	0.037	0.772	80	32.00	1.18	1.88	0.630
3.00	5.00	0.010	0.710	86	31.08	0.31	0.96	0.324



Schematic Tested, ASNS in Use



Notes:
- C2 : can reduce signifigantly
- ASNS Circuit can like be simplified

APPENDIX – *Adding Thermal Foldback* (slide 1 of 3)

TPS92074 Thermal Foldback Testing.

A TPS92074 BUCK Design with output PNP in use can implement a thermal fold back feature with the simple addition of 1 PTC resistor.

The resistor was added as shown in the schematic and test results taken and presented below.
A PTC has a much sharper knee then common NTC's and allows a sharper roll-off with temperature.

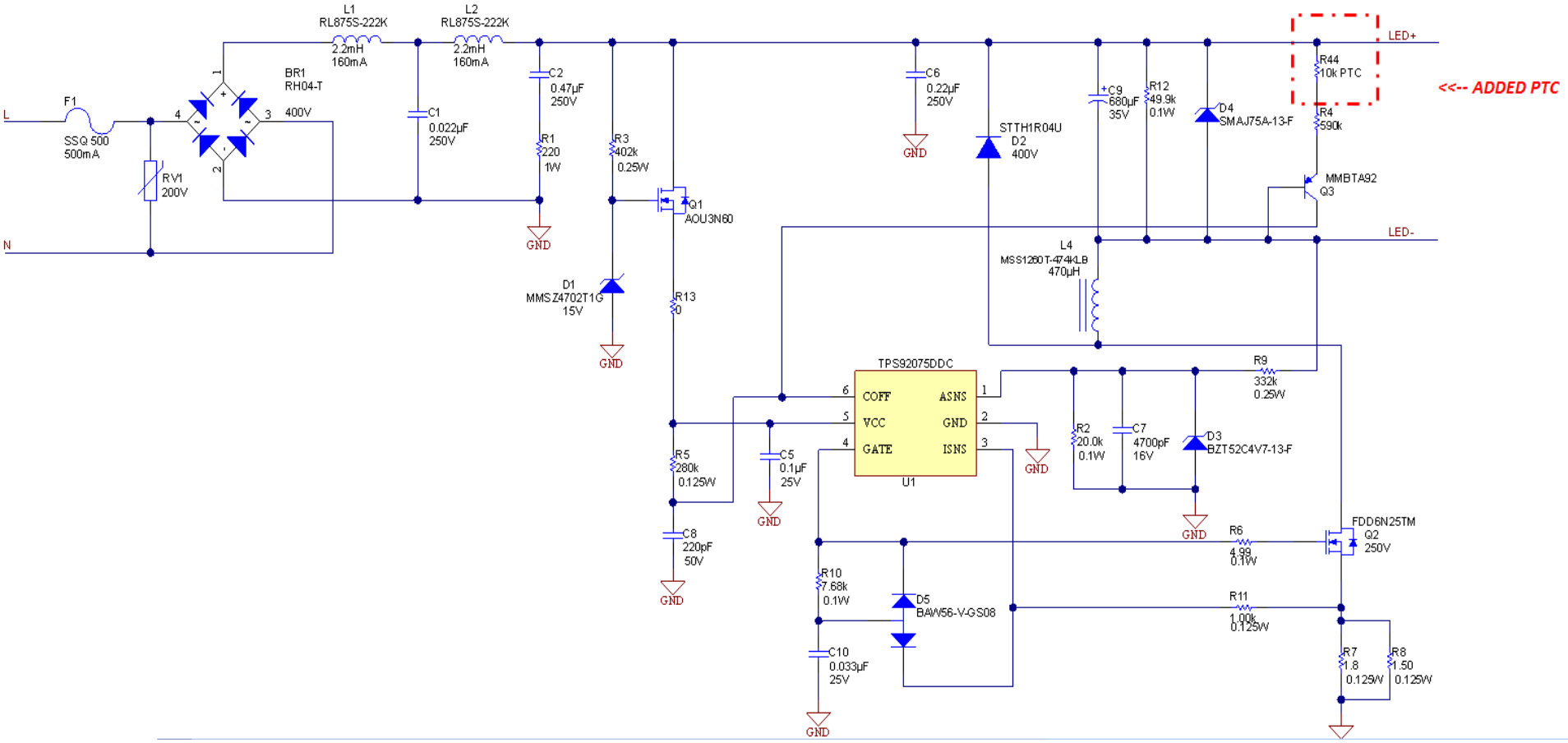
Part Number:
PRF15BG103RB6RC Manufacturer: MURATA

Real Data Curve			
Temperature (°C)	**Current (mA)**	**Voltage (V)**	**Resistance (kΩ)**
25.1	405	28.06	10
29.9	405	27.7	11
33.9	405	27.4	12
39.0	405	27.3	15
44.5	402.3	27.3	20
49.1	398	27.2	27
54.1	394.4	27.2	42
58.7	380.6	27.1	77
63.7	350.2	26.8	168
68.9	294.9	26.2	436
73.8	218.8	25.1	1330
78.9	150	19.6	4700
83.6	55	20.2	15488
88.7	16.08	17.6	52723

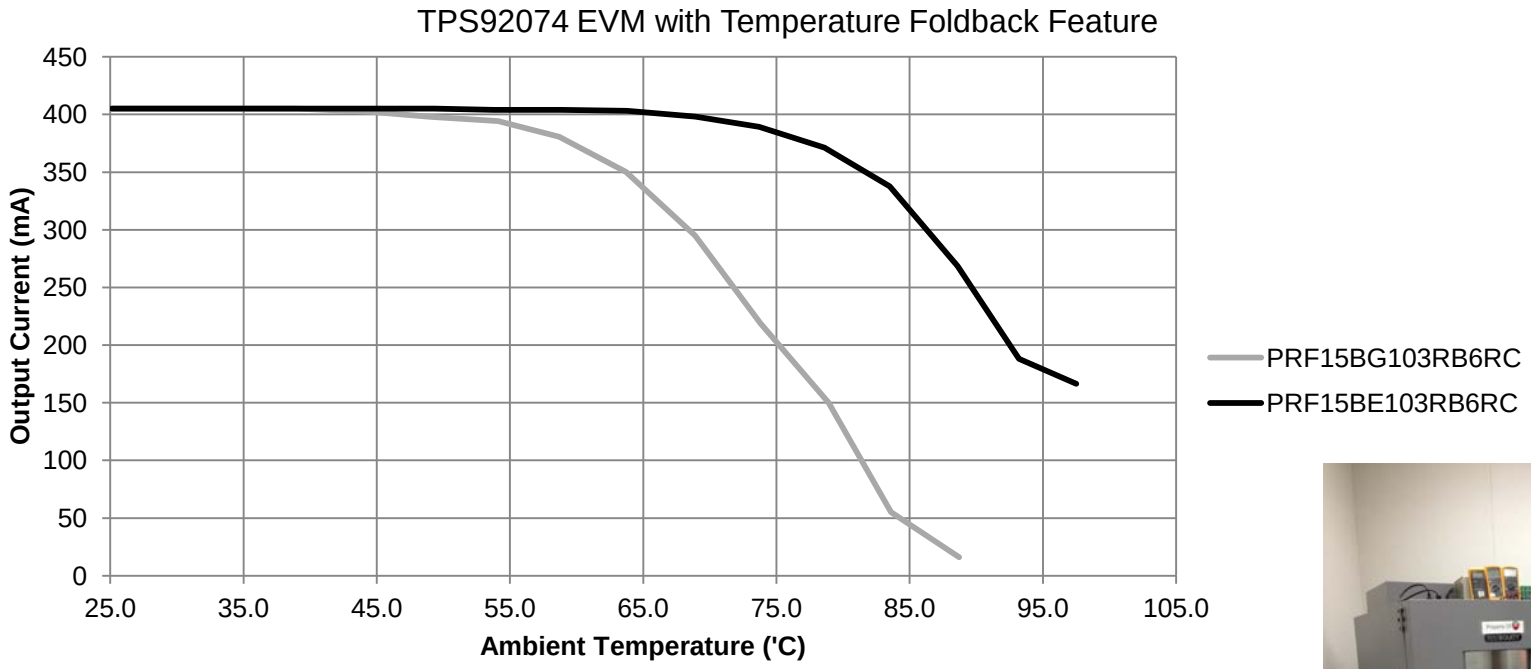
Part Number: PRF15BE103RB6RC Manufacturer: MURATA

Real Data Curve			
Temperature (°C)	**Current (mA)**	**Voltage (V)**	**Resistance (kΩ)**
25.1	405	28.1	10
43.9	405	27.6	11
49.3	405	27.3	12
53.8	404	27.7	14
58.9	404	27.5	17
63.8	403.2	27.4	21
68.9	398.1	27.3	28
73.7	389.2	27.3	46
78.6	371.3	27.1	79
83.5	337.6	26.7	185
88.6	268.5	25.9	434
93.2	188	24.6	1370
97.5	166.5	19.6	4700

APPENDIX – *Adding Thermal Foldback* (slide 2 of 3)



APPENDIX – *Adding Thermal Foldback* (slide 3 of 3)



Test Method: LED driver ambient was taken to noted temperatures, with LEDs external

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