Application Report
SLVAER5–March 2020

TPS92692-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for TPS92692-Q1 (HTSSOP package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 shows the device functional block diagram for reference.

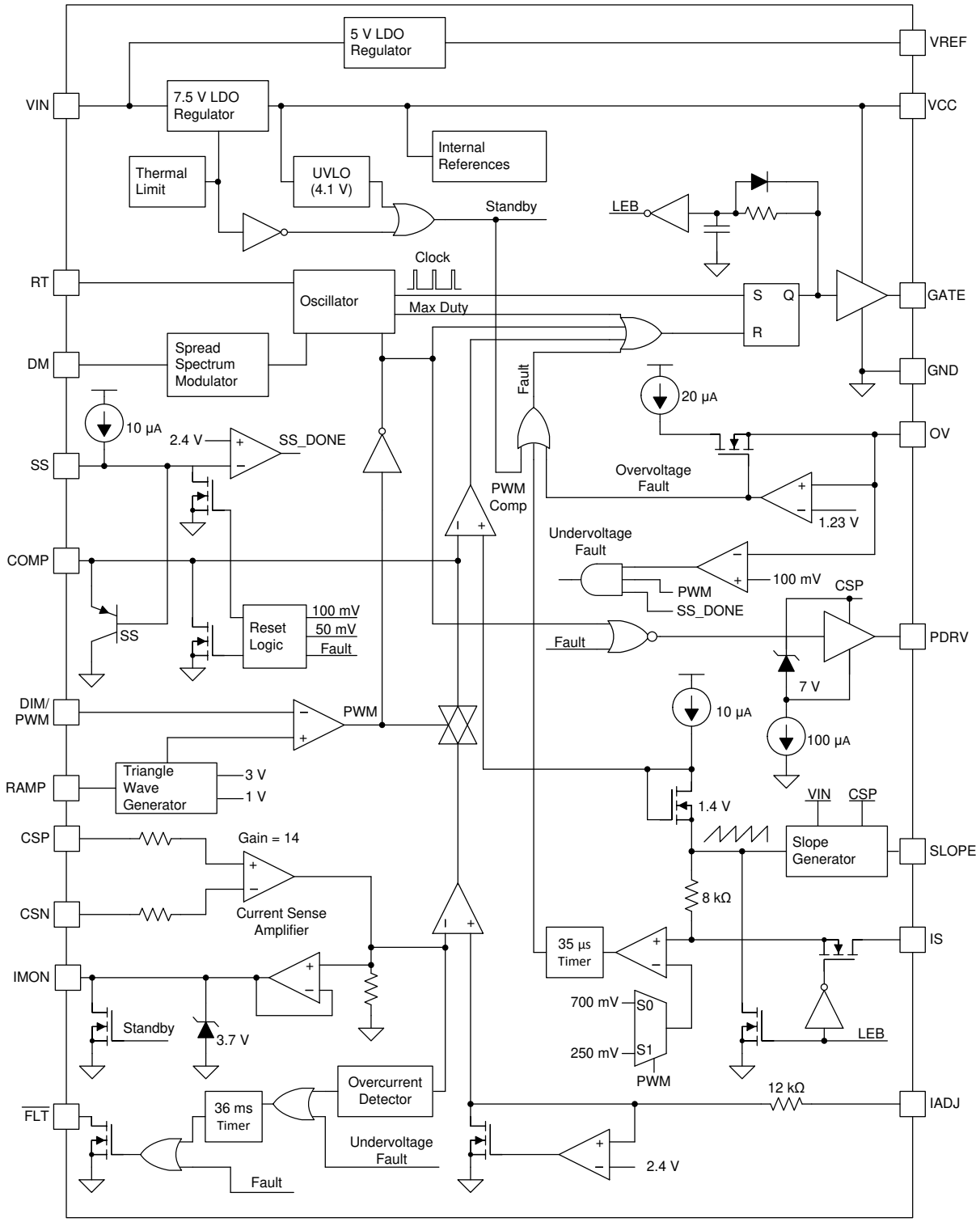

Figure 1. Functional Block Diagram

TPS92692-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS92692-Q1 based on two different industry-wide used reliability standards:

- Table 1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	17
Die FIT Rate	2
Package FIT Rate	15

The failure rate and mission profile information in Table 1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS92692-Q1 in Table 3 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3. Die Failure Modes and Distribution

Die Failure Modes			Failure Mode Distribution (%)
BIAS	VREF-5V_LDO	If IADJ voltage is generated using VREF, ILED will be set to a wrong value	5.7%
	VCC_7.5V_LDO	Internal analog blocks can be damaged or UVLO is triggered	7.5%
	Thermal Limit	Incorrect operation of the Thermal Limit	<0.5%
	UVLO	Incorrect operation of UVLO	1.4%
	Internal References	Device is not functional	6.4%
OSC	Oscillator	Device is not functional or operates at a wrong switching frequency	4.9%
DM	Spread-Spectrum	Spread-Spectrum frequency and magnitude is out of spec.	1.6%
SS	Soft-Start	The part is disabled and doesn't start, or starts with the wrong soft-start slope	1.6%
RAMP	Triangle-Wave-Generator	Incorrect operation of internal PWM	2.1%
SWISNS	Switch Current Sense	Incorrect operation of the device, the device may be unstable	2.8%
SLOPE	Slope Generator	The slope compensation is out of spec, feedback could be unstable	3.7%
GATEDRV	Gate Driver	The output of the Gate Driver can be stuck high or low, causing the main FET to be always ON or OFF	6.5%
FAULT	Over Voltage Fault	Incorrect operation of the OV fault	0.6%
	Fault Logic	Incorrect operation of the fault logic	2.0%
EA_AMP	Error Amplifier	The device regulates the LED current to a higher or lower programmed value, or the device is disabled	2.8%
CSAMP	Current Sense Amplifier	The device regulates the LED current to a higher or lower programmed value, or the device is disabled. IMON does not equal the regulated output	12.4%
PDRV	PFET Driver	External PFET is either fully ON or fully OFF	3.8%
ESD	ESD Cells	PIN may short to GND	34%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS92692-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 5)
- Pin open-circuited (see Table 6)
- Pin short-circuited to an adjacent pin (see Table 7)

Table 5 through Table 7 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4.

Table 4. Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 2 shows the TPS92692-Q1 pin diagram. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the TPS92692-Q1 datasheet.

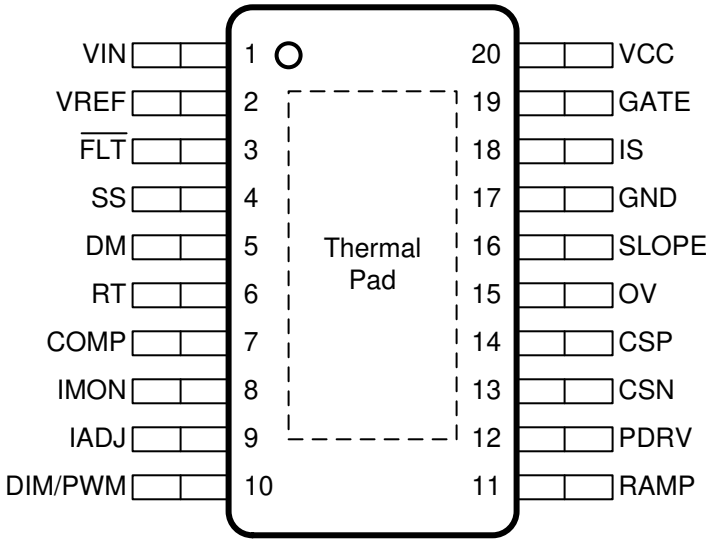

Figure 2. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- There are 8xLEDs connected in series at the output of the device under test.
- BOOST configuration with external PFET PWM dimming is used for the PIN FMA.
- Unless otherwise specified, the voltage applied to the VIN pin is 12 V.

Table 5. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	7	The application and the device will not start	B
CSN	13	In BOOST configuration, this will short VIN to GND and will damage the LED current sense resistor	A
CSP	14	In BOOST configuration, this will short VIN to GND, and may damage external components	A
DIM/PWM	10	The application and the device will not start	B
DM	5	Spread-spectrum is disabled	C
$\overline{\text{FLT}}$	3	If this pin is connected to SS to trigger fault conditions, the application will not start	B
GATE	19	The application will not start	B
GND	17	No effect on the operation of the device	D
IADJ	9	The application will not start	B
IMON	8	LED measurement can not be performed	C
IS	18	Device may operate at max duty cycle and can be damaged	A
OV	15	Over voltage can not be observed, and OV fault is disabled	C
PDRV	12	External PFET is fully ON and can be damaged	A
RAMP	11	PWM dimming can be disabled and the external PFET is fully ON	C
RT	6	Device will not operate	B
SLOPE	16	Depending on the configuration, the device maybe unstable	B
SS	4	The application and the device will not start	B
VCC	20	The application and the device will not operate	B
VIN	1	The application and the device will not operate	B
VREF	2	The application and the device will not operate	B

Table 6. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	7	The device will be out of regulation and unstable, ILIM fault may trigger	B
CSN	13	The LED current is decreased and the device may stop switching	B
CSP	14	ILIM or OV fault may trigger as the output LED current is increased	B
DIM/PWM	10	The application will not start	B
DM	5	The frequency of the spread spectrum increases significantly	C
$\overline{\text{FLT}}$	3	A fault can not be observed on this PIN	C
GATE	19	The application will stop operating	B
GND	17	Device will not operate as expected	B
IADJ	9	LED current will be low; or zero.	B
IMON	8	LED current can not be measured	C
IS	18	Switch current limit may falsely triggered	B
OV	15	The over voltage fault is triggered.	B
PDRV	12	The external PFET is turned off and the LED loads are disconnected from the device. The over voltage fault is triggered.	B
RAMP	11	The internal PWM dimming frequency increases significantly	B
RT	6	Clock period will increase significantly or the device may stop switching	B
SLOPE	16	The application may be unstable	B
SS	4	Faster than normal start-up.	C
VCC	20	The device will not operate as expected	B
VIN	1	Device does not start and will not operate	B
VREF	2	Depending on the operating condition the device may not operate as expected, more noise in the system	B

Table 7. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	VREF	Depending on VIN voltage, part can be damaged. Refer to the ABS MAX table in TPS92692-Q1 datasheet.	A
VREF	2	$\overline{FLT}$	VREF is pulled low initially, which prevents the start-up	B
$\overline{FLT}$	3	SS	No effect on the operation of the device.	D
SS	4	DM	UV function is disabled, TPS92692-Q1 may not operate as expected.	C
DM	5	RT	The switching frequency may slightly change	C
RT	6	COMP	Device will not operate	B
COMP	7	IMON	Device will not operate	B
IMON	8	IADJ	LED current measurement will be inaccurate	C
IADJ	9	DIM/PWM	LED current is increased to the maximum regulation point	C
DIM/PWM	10	RAMP	Corner pin-to-pin short implausible	D
RAMP	11	PDRV	Device can be damaged, refer to the ABS MAX table in TPS92692-Q1 datasheet.	A
PDRV	12	CSN	External PFET is turned off, LED current is decreased to zero, OV fault is triggered	B
CSN	13	CSP	The LED current is initially increased, which causes switch current limit, ILIM, fault to be triggered	B
CSP	14	OV	Device is damaged	A
OV	15	SLOPE	Depending on the configuration, the device maybe unstable	B
SLOPE	16	GND	Depending on the configuration, the device maybe unstable	B
GND	17	IS	Device may operate at max duty cycle and can be damaged	A
IS	18	GATE	Switch current limit, ILIM, fault is triggered at every switching cycle	B
GATE	19	VCC	The external NFET device is fully turned on and can be damaged	A
VCC	20	VIN	Corner pin-to-pin short implausible	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265