**Query**

We are using TPS3431SDRBR Watchdog in our design as shown in the following diagram. The SET1 and WDI pins are controlled by CPU and the CWD pin generates 900 Milliseconds (max.) of Watchdog Timeout (tWD) with 10nF capacitor.

The WDO pin is connected to CPU reset pin POR\_X, and SET1 pins is pulldown.



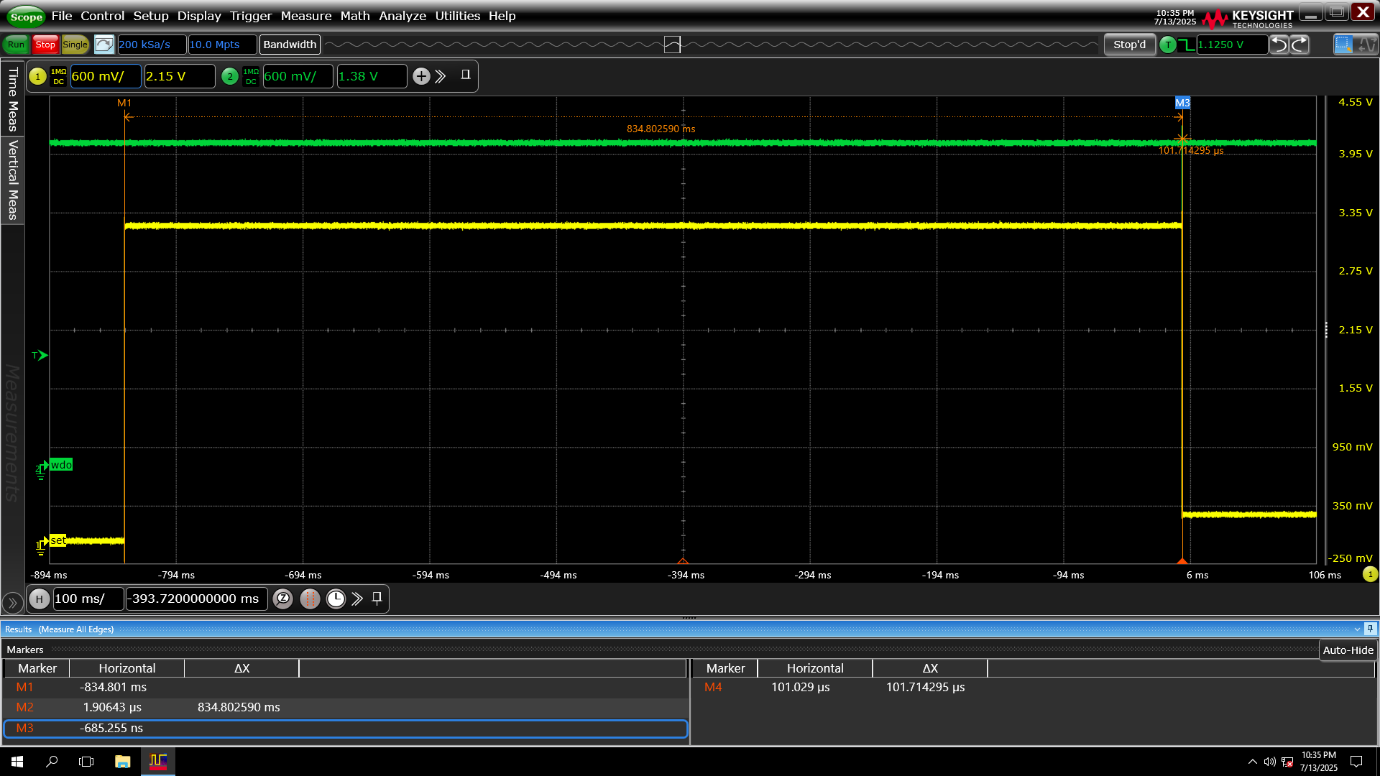
**Test observation:**

The WDT is enabled by making SET1 pin HIGH and WDI pulses are not applied, after 834ms WDO asserts LOW and CPU get reset hence watchdog disabled and due to this reset delay time (TRST) remains Low for 100us only.(Please see below waveforms)

**Q1. With above configuration What is the minimum reset delay time (TRST).**

**Q2. Can it be less than 100us? (Like 1us or 10 us etc.)**

**Waveforms:**



A screenshot of a computer

AI-generated content may be incorrect.