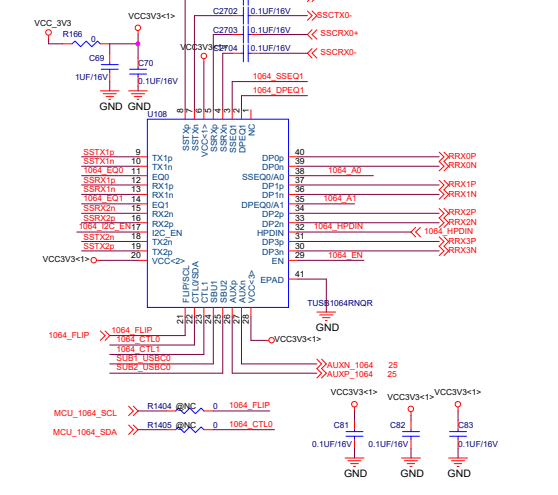
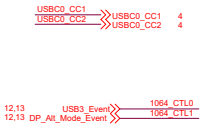
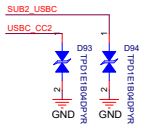
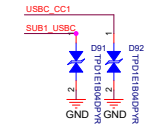
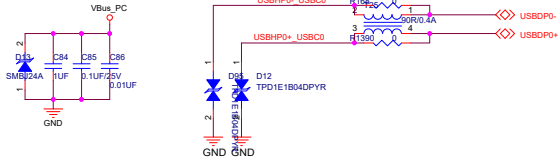
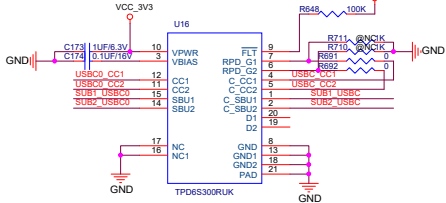
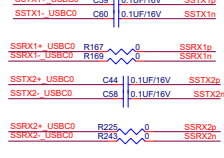
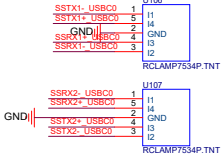
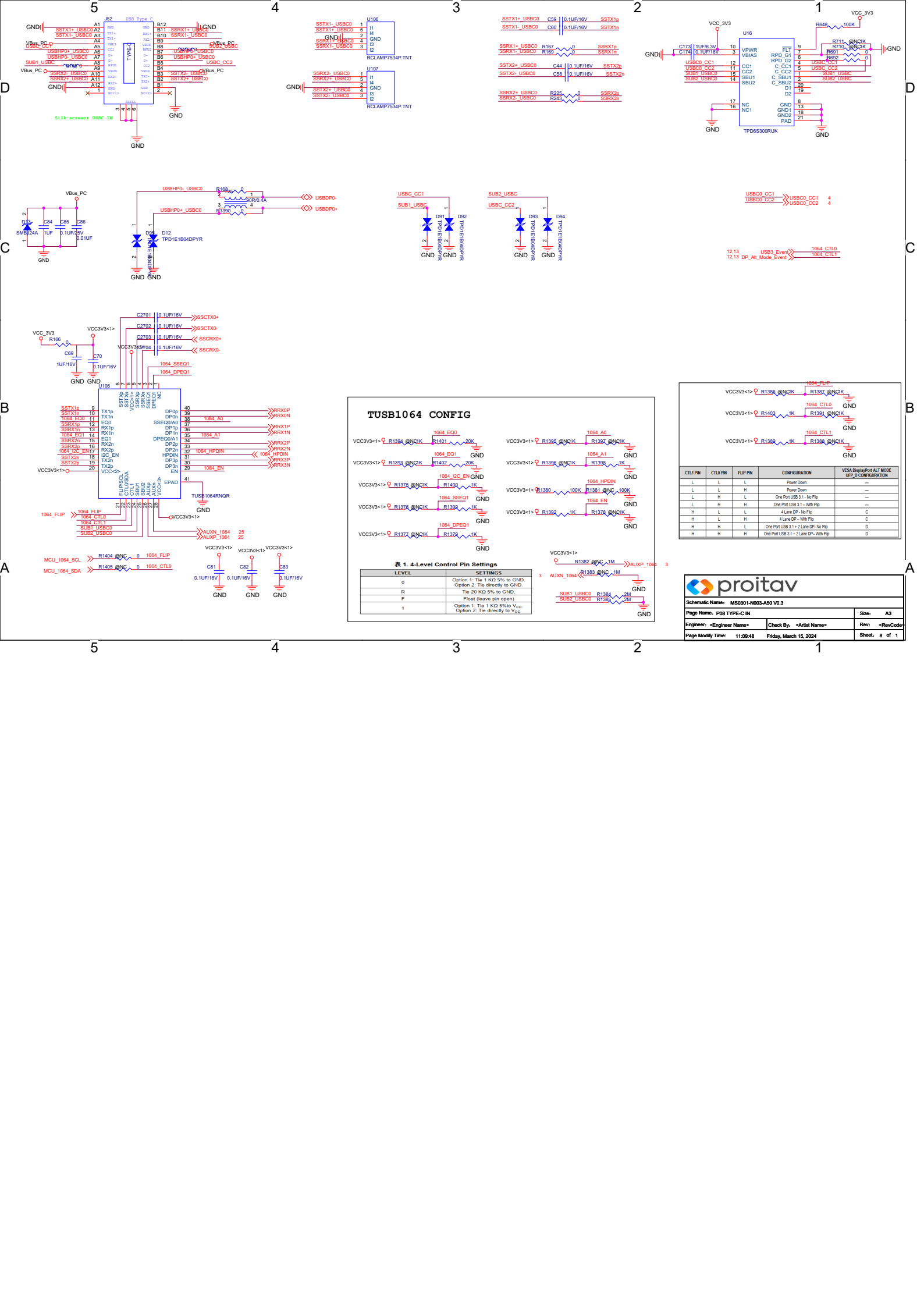


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TUSB1064 CONFIG

VCC3V3<1> Q R139A @NCK R1401 20K

VCC3V3<1> Q R139B @NCK R1402 20K

VCC3V3<1> Q R137A @NCK R1400 1K

VCC3V3<1> Q R137B @NCK R1398 1K

VCC3V3<1> Q R137C @NCK R1378 1K

VCC3V3<1> Q R137D @NCK R1377 1K

VCC3V3<1> Q R1382 @NCK R1381 100K

AUXN_1064 R1383 @NCK 1M

SUB1_USBC R1384 2M

SUB2_USBC R1385 2M

MCU_1064_SCL R1404 @NCK 0 1064_FLIP

MCU_1064_SDA R1405 @NCK 0 1064_CTL0

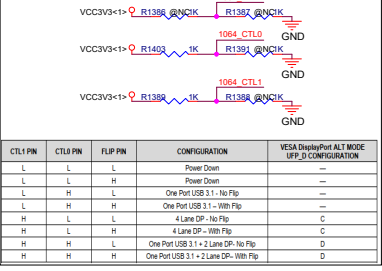
VCC3V3<1> C81 0.1UF16V

VCC3V3<1> C82 0.1UF16V

VCC3V3<1> C83 0.1UF16V

表 1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Option 1: Tie 1 KΩ 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 KΩ 5% to GND.
F	Float (leave pin open).
1	Option 1: Tie 1 KΩ 5% to V _{CC} . Option 2: Tie directly to V _{CC} .



CTL1 PIN	CTL0 PIN	FLIP PIN	CONFIGURATION	VESA DisplayPort ALT MODE UFP_D CONFIGURATION
L	L	L	Power Down	—
L	H	L	Power Down	—
L	H	H	One Port USB 3.1 - No Flp	—
L	H	H	One Port USB 3.1 - With Flp	—
H	L	L	4 Lane DP - No Flp	C
H	L	H	4 Lane DP - With Flp	C
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flp	D
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flp	D

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Size: A3

Engineer: <Engineer Name> Check By: <Artist Name> Rev: <RevCode>

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