# BQ76952EVM Test Results

Test conditions:
BQ76952EVM with 4 LFP Cells, with and without 100 Ohm load resistance

| Test  | Load | ALL\_FETS\_ON Command | Steps | PDSG Behavior | PACK VOLTAGE Behavior |
| --- | --- | --- | --- | --- | --- |
| 1 | 100 Ohm | Present | 1. Set PDSG TIMEOUT to 2 Sec2. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 05. Send ALL\_FETS\_ON | Asserted, then de-asserted after 2 sec | 0.32V → 12.29V after 2 sec |
| 2 | 100 Ohm | Present | 1. Set PDSG STOP DELTA to 2552. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 05. Send ALL\_FETS\_ON | Remains asserted | Stays at 0.32V |
| 3 | 100 Ohm | Absent | 1. Set PDSG TIMEOUT to 2 Sec2. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 0 | Asserted, then de-asserted after 2 sec | 0.32V → 12.29V after 2 sec |
| 4 | 100 Ohm | Absent | 1. Set PDSG STOP DELTA to 2552. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 0 | Remains asserted | Stays at 0.32V |
| 5 | No Load | Absent | 1. Set PDSG TIMEOUT to 2 Sec2. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 0 | Asserted, then de-asserted after 2 sec | 0.32V → 12.29V after 2 sec |
| 6 | No Load | Absent | 1. Set PDSG STOP DELTA to 2552. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 0 | Asserted, then de-asserted | 12.41V → 12.53V |
| 7 | No Load | Present | 1. Set PDSG TIMEOUT to 2 Sec2. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 05. Send ALL\_FETS\_ON | Asserted, then de-asserted after 2 sec | 12.41V → 12.53V |
| 8 | No Load | Present | 1. Set PDSG STOP DELTA to 2552. Set DFETOFF to 13. Send ALL\_FETS\_OFF 4. Set DFETOFF to 05. Send ALL\_FETS\_ON | Remains asserted | Stays at 12.41V |

Test 1: PDSG Timeout 2000 ms
Source1: Stack Voltage
Source2: LD Voltage


Test 1: PDSG Timeout 2000 ms
Source1: DSG
Source2: LD\_Voltage


Test 1: PDSG Timeout 2000 ms
Source1 PDSG
Source2: LD\_Voltage


Test 2: PDSG stop delta 255 (=2.55 V)
Source1: Stack Voltage
Source2: LD Voltage


Test 2: PDSG stop delta 255 (=2.55 V)
Source1: DSG
Source2: LD Voltage


Test 2: PDSG stop delta 255 (=2.55 V)
Source1: PDSG
Source2: LD Voltage



Test 4: PDSG Timeout 2000 ms (No Load)
Source1: Stack Voltage
Source2: LD Voltage

Test 4: PDSG Timeout 2000 ms (No Load)
Source1: DSG
Source2: LD Voltage



Test 5: PDSG stop delta 255 (=2.55 V) (No Load)
Source1: Stack Voltage
Source2: LD Voltage


Test 5: PDSG stop delta 255 (=2.55 V) (No Load)
Source1: DSG
Source2: LD Voltage

