Application Note

UCC25640x Application Debug FAQs

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ABSTRACT

This application note discusses the UCC25640x LLC resonant controller's most frequently asked questions when used in different applications.

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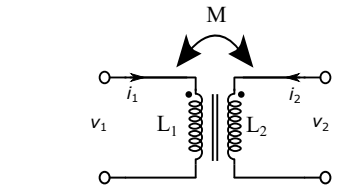
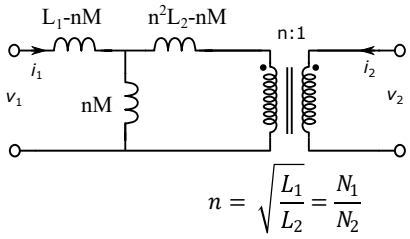
1 UCC25640x Frequently Asked Questions

1.1 The recommended LLC transformer models for both time domain simulation and fundamental harmonic analysis

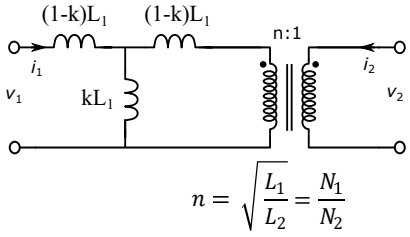
The LLC topology can be realizable with a. an external inductor and a tightly coupled transfomer or b. with a integrated transformer with a poor coupling which integrates both resonant and magnetizing indcutors. In both of these implementations, the transfomer can be modelled as T-type [1] or APR models which are shown in Figure 1-1. These two models can be used for both time domain simulation and also for fundamental harmonic analysis. Equation 1, Equation 2, Equation 3 describe the behaviour of all the models given in Figure 1-1. Reference [2] shows the different transformer model derivations from a mutual inductance transformer model.



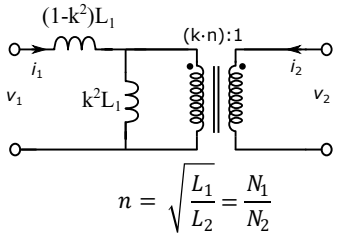
a. Mutual Inductance model



b. T type Transformer model



c. T type Transformer model considering coupling coefficient k



d. All Primary Referred (APR) model

Figure 1-1. Tranformer models

$$v_1 = L_1\frac{di_1}{dt} + M\frac{di_2}{dt} \quad (1)$$

$$v_2 = L_2\frac{di_2}{dt} + M\frac{di_1}{dt} \quad (2)$$

$$k = \frac{M}{\sqrt{L_1 L_2}} \tag{3}$$

where L_1, L_2, M, k are primary open circuit Inductance, Secondary open circuit indcutance, Mutual Inductance, coupling coeffcient respectively.

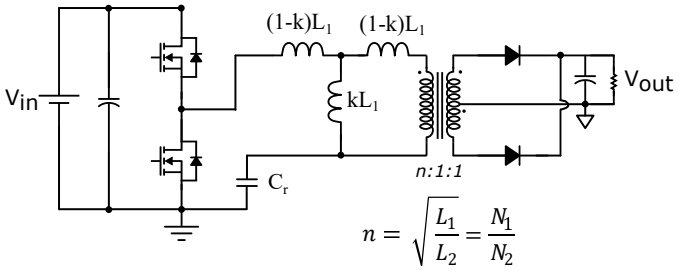


Figure 1-2. T-type transformer model for LLC Design and Analysis

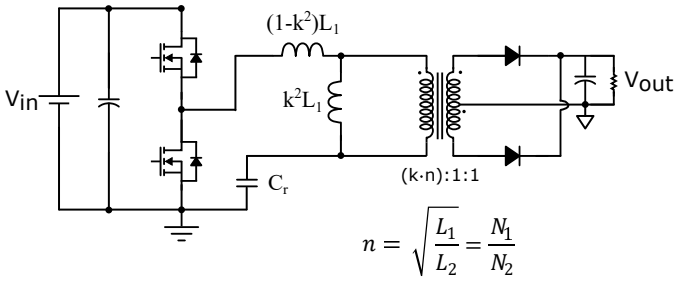


Figure 1-3. APR-type transformer model for LLC Design and Analysis

The parameters of the models shown in Figure 1-1 can be calculated from the transformer datasheet parameters where primary open circuit Inductance (L_p) and primary inductance when secondaries are short (L_{lk}), turns ratio are given.

$$k = \sqrt{1 - \frac{L_{lk}}{L_p}} \tag{4}$$

$$L_1 = L_p \tag{5}$$

$$n = \text{turns ratio} \tag{6}$$

To validate models, a closed loop simplis simulation with both T-type model shown in Figure 1-2 and APR model shown in Figure 1-3 has been built with the same transformer parameters as that of UCC25640x EVM hardware [3] where integrated transformer from Wurth Electronics [4] is used. In the transformer datasheet, L_p, L_{lk}, n are given as 510uH, 82uH, 16.5 respectively. From Equation 4, Equation 5, Equation 6, the parameters of the transfomer obtained as k =0.916, L_1=510uH, n=16.5, k*n=15.115. Figure 1-4 shows the comparison between EVM measurements and closed loop Simplis models. We can observe that in all the cases the operating frequency is almost same for a given input voltage.

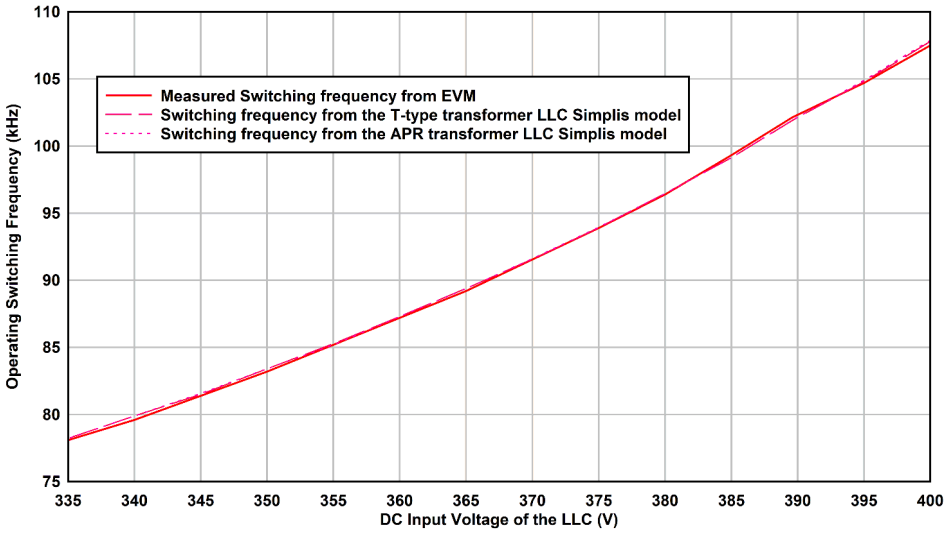


Figure 1-4. Input voltage vs switching frequency from closed loop time domain simulation models and from the EVM measurements at 12V,15A load

1.2 LLC resonant circuit parameters design example (UCC25640EVM-020) with Integrated Transformer based on FHA

1.2.1 Fundamental Harmonic model of the LLC with T-type transformer model and voltage gain vs frequency relationship

The contents of this section are taken from the reference [1].

Figure 1-5 shows the fundamental harmonic model of the Figure 1-2. As explained in the Section 1.1, L_1, k of the Figure 1-5 can be derived from transformer data sheet using Equation 4, Equation 5, Equation 6 .

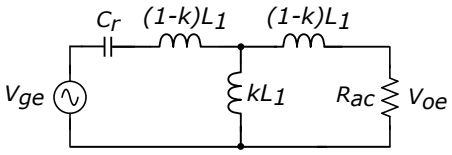


Figure 1-5. LLC linear sinusoidal model

Equation 7 shows the relation between output and input voltages of the Figure 1-2 and Figure 1-5.

$$\frac{2 \cdot n \cdot V_{out}}{V_{in}} \approx M = \frac{V_{oe}}{V_{ge}} \tag{7}$$

where

$$\text{Voltage Gain: } M(k, fr, Q) = \frac{1}{\sqrt{\left[\frac{1}{k}\left[1 - \frac{1-k^2}{fr^2}\right]^2\right]^2 + \left[\frac{1}{k \cdot Q}\left[fr - \frac{1}{fr}\right]\right]^2}} \tag{8}$$

$$\text{Normalized frequency: } fr = \frac{\omega}{\omega_0} \tag{9}$$

$$\text{Angular resonant frequency between leakge inductance (primary-side inductance when the secondary side is completely short-circuited) and Cr: } \omega_0 = \frac{1}{\sqrt{L_{lk} \cdot C_r}} \tag{10}$$

$$\text{Angular resonant frequency between primary inductance (self-inductance of the primary winding) and Cr: } \omega_s = \frac{1}{\sqrt{L_p \cdot C_r}} \tag{11}$$

$$\text{characteristic impedance: } Z_0 = \sqrt{\frac{L_{lk}}{C_r}} \tag{12}$$

$$\text{Quality factor: } Q = \frac{R_{ac}}{Z_0} = \frac{8 \cdot n^2}{\pi^2} \cdot \frac{R_L}{Z_0} \tag{13}$$

n : primary to secondary turns ratio (14)

k : Coupling coeffcient between primary and secondary winding of the transformer (15)

Using Equation 8 , gain plot curves are drawn for different coupling coefficients which is shown in Figure 1-6.

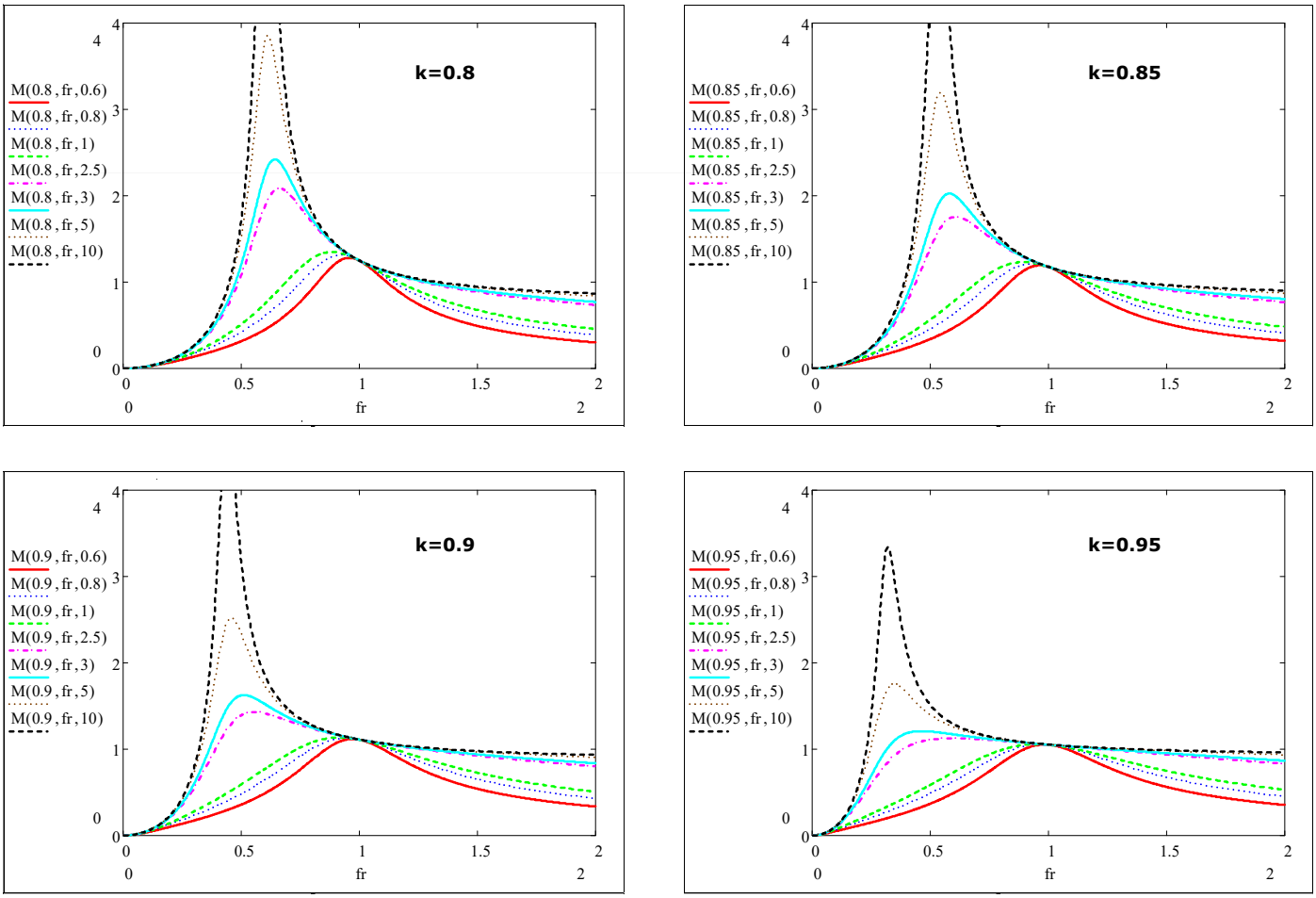


Figure 1-6. Gain frequency plots for different coupling coefficients

1.2.2 UCC25640EVM-020 LLC resonant circuit parameters design example

Table 1-1. UCC25640EVM-020 Specifications

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	INPUT CHARACTERISTICS					
	DC voltage range		365	390	410	VDC
	AC voltage range		85		265	VAC
	AC voltage frequency		47		63	Hz
	Input DC UVLO On			365		VDC
	Input DC UVLO Off			330		VDC
	OUTPUT CHARACTERISTICS					
V_{OUT}	Output voltage - Normal mode	Burst mode threshold to full load = 15 A		12		VDC
I_{OUT}	Output load current	365 to 410 VDC			15	A
	Output voltage ripple	390 VDC and full load = 15 A		120		mVpp
	SYSTEM CHARACTERISTICS					
	Resonant frequency			100		kHz
	Peak efficiency	390 VDC, load = 8 A		93%		
	Operating temperature	Natural convection		25		°C

Nominal Input Voltage: $V_{in\_Nom} = 390V$ (16)

Output Voltage: $V_{out} = 12V$ (17)

Nominal Output Power: $P_{out} = 180W$ (18)

Output Voltage ripple: $120mVpp$ (19)

Voltage drop due to power losses: $V_{loss} = \frac{\frac{180W}{93\,\%} \cdot 7\,\%}{15A} = 0.9V$ (20)

Coupling coefficient considered for this design: $k = 0.92$ (21)

Gain at the resonant frequency: $M_{fo} = \frac{1}{k} = 1.087$ (22)

Primary to Secondary turns ratio: $n = M_{fo} \cdot \frac{V_{in\_Nom}}{2 \cdot (V_{out} + V_{loss})} \cong 16.5$ (23)

Equivalent Output Load Resistance: $R_L = \frac{12V^2}{180W} = 0.8\Omega$ (24)

Equivalent AC Load Resistance: $R_{ac} = \frac{8 \cdot n^2}{\pi^2} \cdot R_L = 176.542$ (25)

Minimum DC Input Voltage: $V_{in\_\min} = 365V$ (26)

Maximum DC Input Voltage: $V_{in\_\min} = 410V$ (27)

Maximum gain requirement: $M_{\max} = \frac{2n \cdot (V_{out\_\max} + V_{loss})}{V_{in\_\min}} = \frac{2 \cdot 16.5 \cdot (12 + 0.06 + 0.9)}{365} = 1.172$ (28)

Minimum gain requirement: $M_{\min} = \frac{2n \cdot (V_{out\_\min} + V_{loss})}{V_{in\_\max}} = \frac{2 \cdot 16.5 \cdot (12 - 0.06 + 0.9)}{410} = 1.033$ (29)

Quality factor of 3.5 is considered for this design.

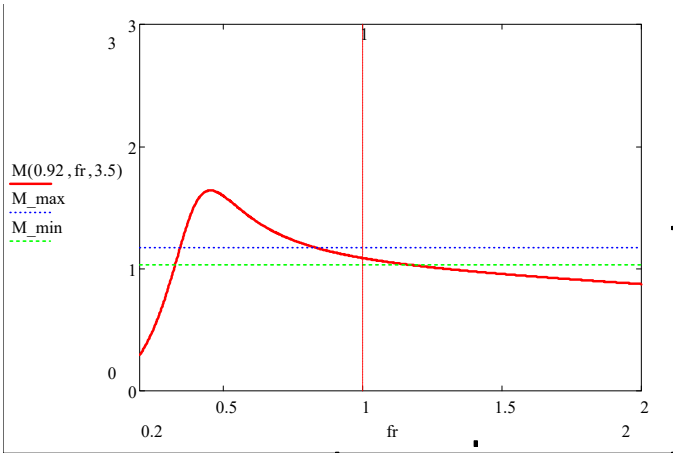


Figure 1-7. Gain frequency plot for k=0.92 and Q=3.5

Characteristic Impedance: $Z_0 = \frac{R_{ac}}{Q} = \frac{176.542}{3.5} = 51.5$ (30)

Resonant Frequency: $f_o = 100kHz$ (31)

Resonant Capacitor Value: $C_r = \frac{1}{2\pi \cdot Z_0 \cdot f_o} = 31.5nF$ (32)

Primary Leakage Inductance when the secondaries are short circuited: $L_{lk} = \frac{Z_0}{2\pi f_o} = 80\mu H$ (33)

Primary Inductance when the secondaries are open circuited: $L_p = \frac{L_{lk}}{1 - k^2} = 522\mu H$ (34)

Final value of resonant capacitor value selected: $C_r = 30nF$ (35)

Leakage Inductance, primary Inductance, turns ratio values given in the transformer data sheet: $L_{lk} = 82\mu H, L_p = 510\mu H, n = 16.5$ (36)

The final resonant frequency: $f_0 = \frac{1}{2\pi\sqrt{L_{lk} \cdot C_r}} = 101.5kHz$ (37)

1.3 How to connect external gate drivers to the UCC25640x for high gate driver current capability?

Figure 1-8 shows a simpler way of connecting external gate drivers to the UCC25640x. Here two low-side drivers such as UCC27517A [5] is used which has a higher output current capability. Here the external high side driver is bootstrapped just like the internal driver of the UCC25640x.

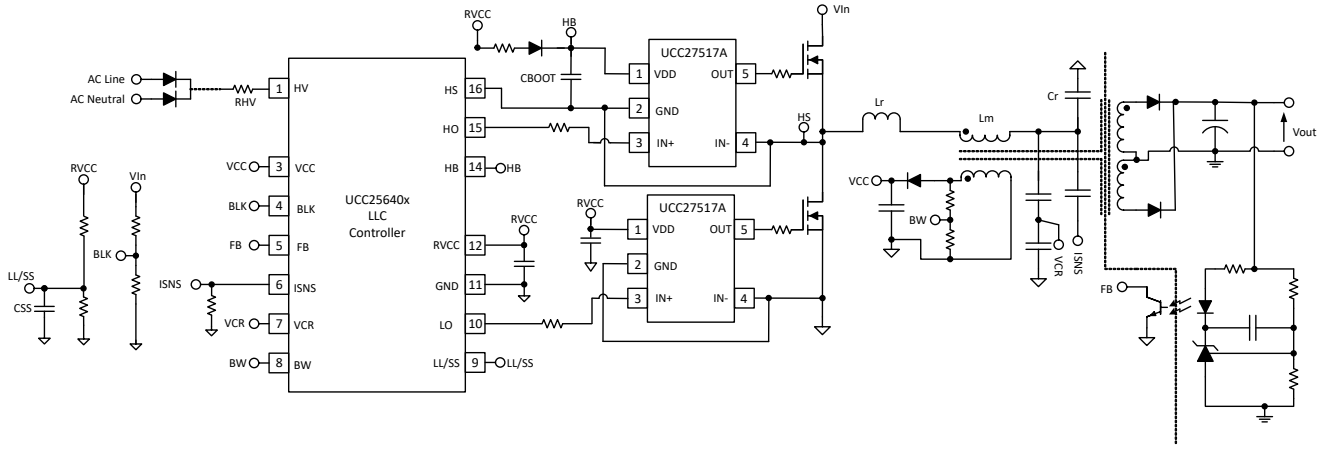


Figure 1-8. External Driver interface to the UCC25640x

1.4 What is the recommended power on sequence of the PFC and LLC Converters?

Normally, LLC can start switching before the PFC output voltage starts rising or vice versa depending on system requirement.

In general, PFC output voltage will start raising before the LLC converter starts switching. Doing so, we are allowing a lower current stress during the startup. UCC25640x RVCC is designed for this purpose. In case of UCC256402/404, once the AC input is provided and VCC reaches 26V level, RVCC voltage is generated to power up PFC controller for PFC to boost. Once PFC boost to a level above UCC25640x BLK setting, LLC DC-DC start to operate. For any reason, if the BLK voltage reaches below BLKstop, switching stops.

In case of TVs, during light load, LLC converter need to startup before PFC output voltage rises. In this kind of scenario, UCC256404 is recommended, since the BLK turn on threshold of this controller is only 1V. Since LLC transformer was designed for input voltage>300V and full load, there won't be any issue of triggering OCP protection.

1.5 How to eliminate the nuisance ZCS detection during the light load?

During light load, the magnitude of resonant current will be very small during the turn off of high side or low side MOSFET. This can trigger the ZCS protection.

Following methods helps to avoid nuisance ZCS detection during light load:

1. Increasing the burst mode threshold (BMTH): ZCS is disabled If we make FBreplica<BMTH during light load.
2. Reducing the magnetizing inductance of the transformer to increase the magnetizing current at light load.
3. Reducing the bypass capacitor on ISNS pin

1.6 Why the UCC25640x controllers FB pin voltage maintained at constant voltage? Add figure FBpin voltage and current, Iout and Vout

The UCC25640x controller attempts to loosely regulate the FB pin voltage to around 5.6V. This is done to provide better transient response and avoid some of the delays associated with the opto-coupler being saturated. When a current pulled out of the FB pin is within 0uA to FB pin maximum source current (164 uA for 402 and 404 devices, 246 uA for 403), the FB pin voltage will be around 5.6V. When the opto-coupler pulls more current than the FB pin can support, the controller will allow the FB pin voltage to collapse to 0V.

1.7 How to improve the slew rate detection at HS pin?

UCC25640x has a minimum detectable slew rate of 100 mV/ns. If the slew rate is detected (this is checked when the switch node voltage is close to 20 V), next gate will be turned on immediately. If the slew rate detection is missed, the dead time would be set as 1.1us. Figure 1-9 shows a way of extracting slew rate information during the dead time [10]. In this simulation Infineon IPW6075CP MOSFET is used. Figure 1-10 shows the switch node volatge transition when a current of 0.7A is being pulled out from switch node. Here we can observe that switch node voltage has different slew rates during the transition which is due to non linear capacitance seen at the switch node as shown in Figure 1-14 (This capcaitance is the combination of Coss of the both upper (voltage changing from 0 to 390) and lower (voltage changing from 390 to 0) MOSFETs shown in Figure 1-12 and Figure 1-13). This graph is extarcted using the SIMetrix simulation shown in Figure 1-11.

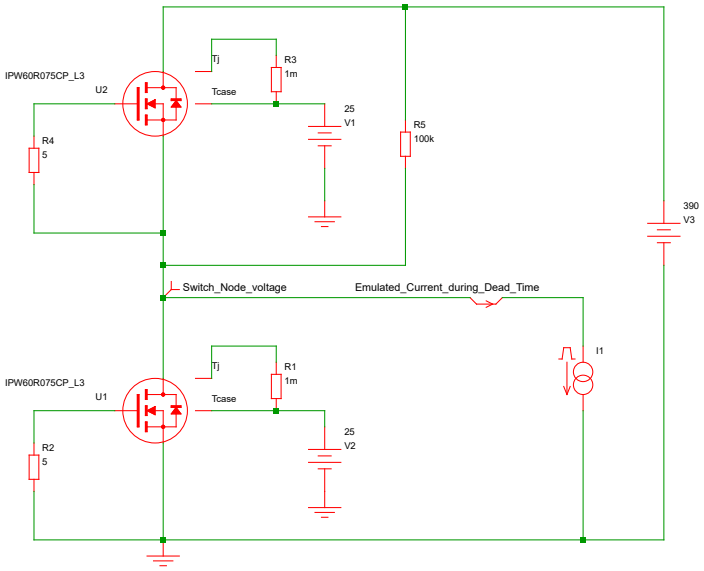


Figure 1-9. SIMetrix simulation for finding switch node slew rate during dead time

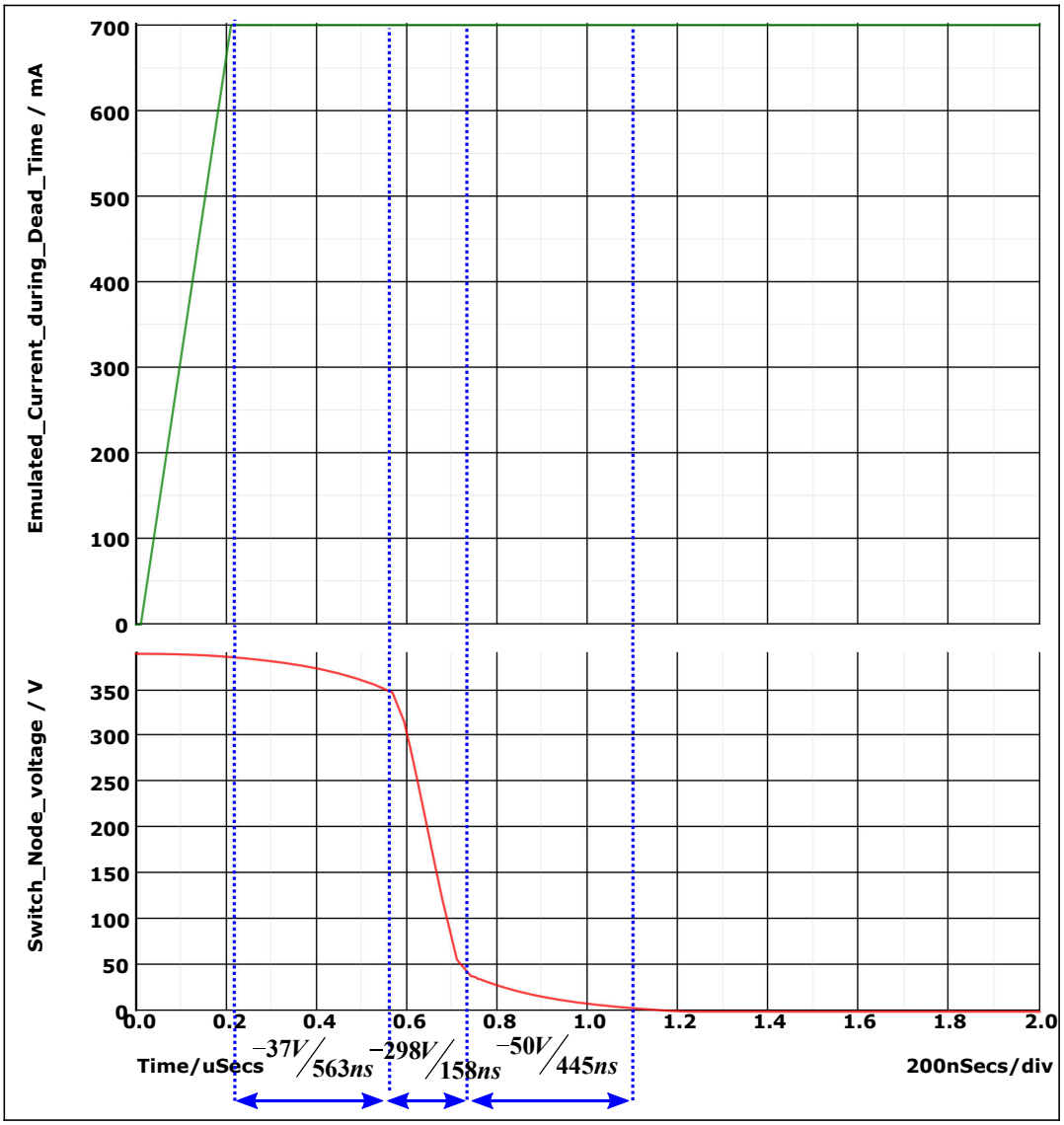


Figure 1-10. Switch node voltage slew rates during dead time

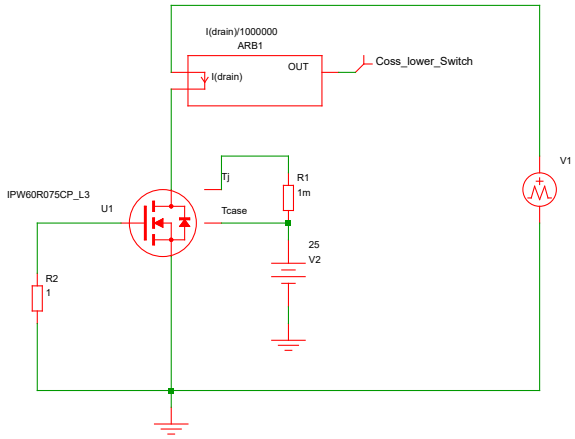


Figure 1-11. Coss extraction from device model using SIMetrix

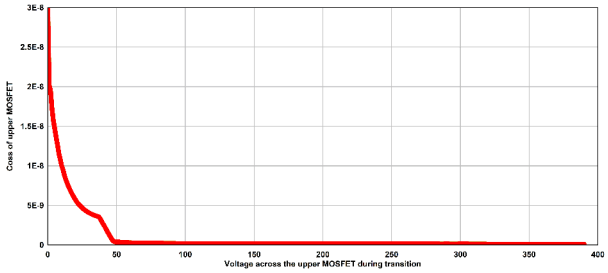


Figure 1-12. Upper MOSFETs Coss vs Drain to Source voltage

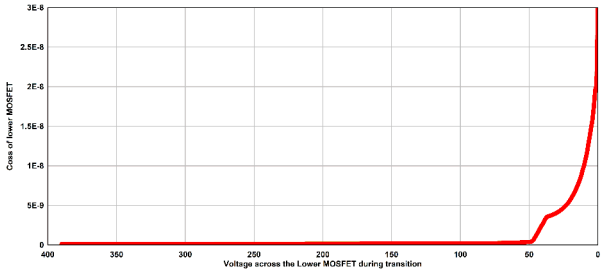


Figure 1-13. Lower MOSFETs Coss vs Drain to Source voltage

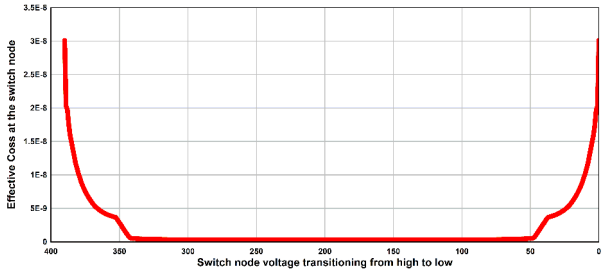


Figure 1-14. Coss seen at the switch node vs switch node voltage

Following methods can be followed to improve the slew rate detection:

1. Increase the MOSFET turn off speed: Most designs include a diode in the HO/LO gate drive paths to allow for independent turn on and turn off speed. Such a circuit is recommended to increase the turn off speed of the gate drive.
2. Using MOSFETs with lower output capacitance (Coss): The lower Coss will allow for a faster switch node slew rate.
3. Using a higher burst mode setting: A higher burst mode setting will have larger magnetizing current amplitude which will help with achieving the dV/dt criteria (Increasing the burst threshold will make the LLC burst with slightly more power within the burst packet and the resonant current amplitude will be higher. This increases the slew rate of the switch node as well)
4. Reducing any snubber capacitance on the switch node
5. Reducing the magnetizing inductance of the transformer to increase the magnetizing current at light load.

1.8 How to operate the UCC25640x controller in the open loop? add waveform

Running UCC25640x open loop would require some modifications to the VCR circuitry as well as the FB pin to sink a constant current out of the FB pin. Since the FB pin is loosely regulated to ~5.6V, connecting a resistor (R_{FB}) from FB to ground sinks a fixed current (somewhere between 0uA and 82uA). The amount of current would determine the switching thresholds ((V_{TH}-V_{TL}) =$V_{vcr\_pk\_pk}$) for VCR. And then depopulate the top VCR capacitance so that charge control is completely disabled. Now the switching frequency (f_{sw}) is only dependent on the internal 2mA ramp current and the lower VCR capacitance (C_{VCR_lower}).

$$\text{The amount of current sunk out of the FB pin: } I_{FB\_pin} = \frac{V_{FB}}{R_{FB}} = \frac{5.6}{R_{FB}} \tag{38}$$

$$\text{VCR peak to peak voltage: } V_{vcr\_pk\_pk} = (82\mu A - I_{FB\_pin}) \cdot 100k\Omega \tag{39}$$

$$\text{Switching frequency: } f_{sw} = \frac{2mA}{2 \cdot V_{vcr\_pk\_pk} \cdot C_{VCR\_lower}} \tag{40}$$

1.9 What happens if the VCR pin peak to peak voltage of the controller exceeds 6V?

VCR pin voltage is internally clamped. It won't go above +7V or below -0.8V. 7V is the internal AVDD rail that powers the VCR circuitry. At -0.8V, the internal ESD diode will likely conduct. VFBreplica peak to peak is clamped to 6V. If the amplitude on the VCR pin exceeds 6V peak to peak, the controller is unable to push the

switching frequency any lower because it has run out of room on VCR and as a result, the converter will get clamped to this minimum switching frequency and the output voltage will droop. If the peak to peak voltage on VCR exceed 6V, try reducing the top VCR capacitor or increase the bottom VCR capacitor to reduce the peak to peak voltage.

1.10 What parameters of UCC25640x that impact the startup duration of the LLC?

In general, the soft start profile of the LLC is normally fine-tuned on bench by adjusting the LL/SS soft start capacitance, soft start initial voltage, VCR capacitors, and feedback loop response. Section 2 of the UCC25630x practical design guidelines [7] gives more details on soft start timing and switching frequency tuning during the startup.

1.11 What causes the current imbalance in the secodary side windings of the LLC?

In the LLC center tapped transformer, If the primary to secondaries leakage inductances are different, we would observe that secondary peak currents will be different during each half of the switching period. This can cause one of the diodes overheating. To avoid this both the windings has to be tightly coupled with the primary so that leakage inductance variation is very small between the windings.

To see the current imbalance on the secondary side, two simulations are considered. Case one: With the equal coupling between primary and secondary windings which is shown in Figure 1-15 (This figure shows all the T-type equivalent models) and Case 2: With the unequal couplings which is shown in Figure 1-16. The EVM parameters are used for both the simulations: k =0.916, L_1=510uH, n=16.5, C_r=30nF, f_{sw}=101.5kHz, Load Resistance=0.8 Ohm. We can observe the seondary side currents imbalance in Figure 1-18 compared to Figure 1-17.

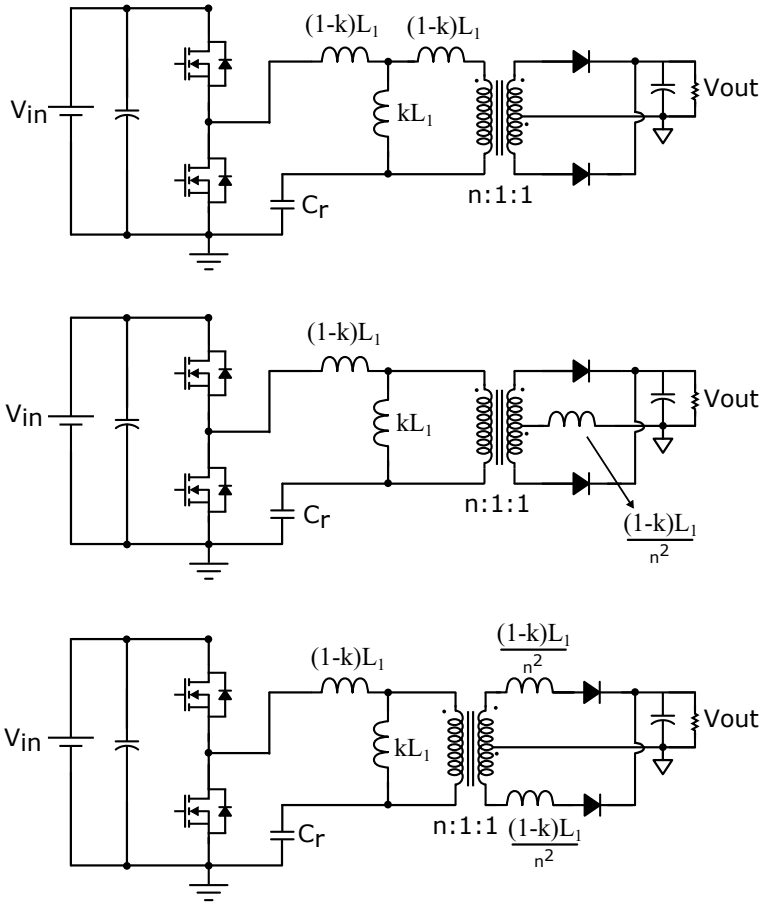


Figure 1-15. LLC T-type equivalent models

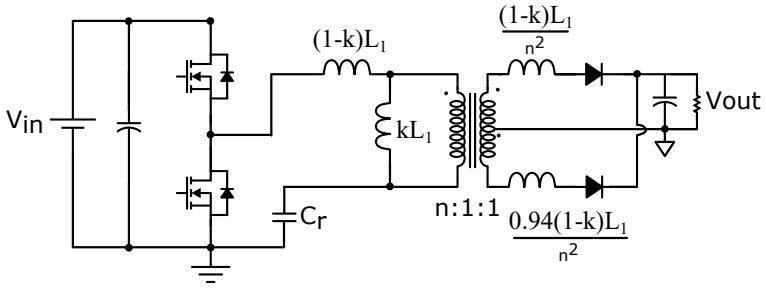


Figure 1-16. LLC Transfomer with unequal coupling

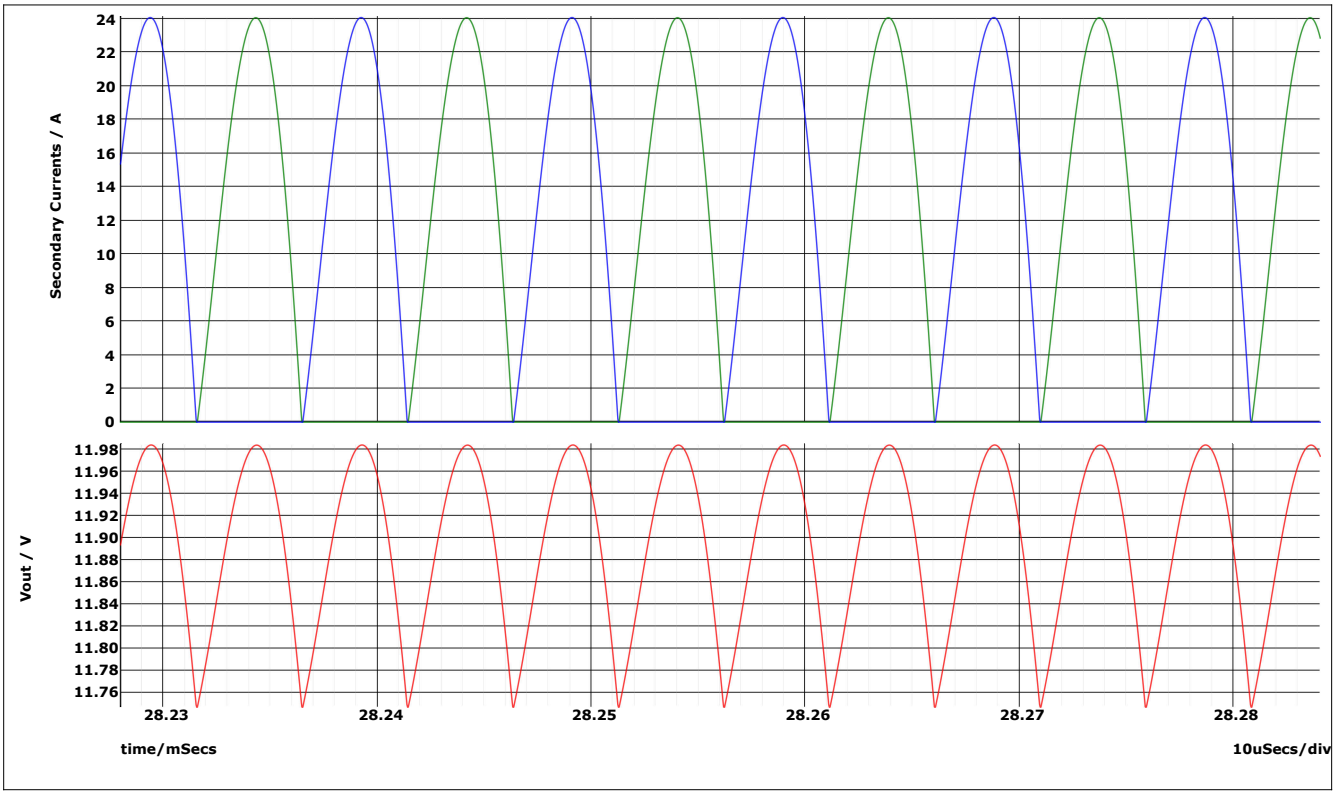


Figure 1-17. Case 1 Simulation results

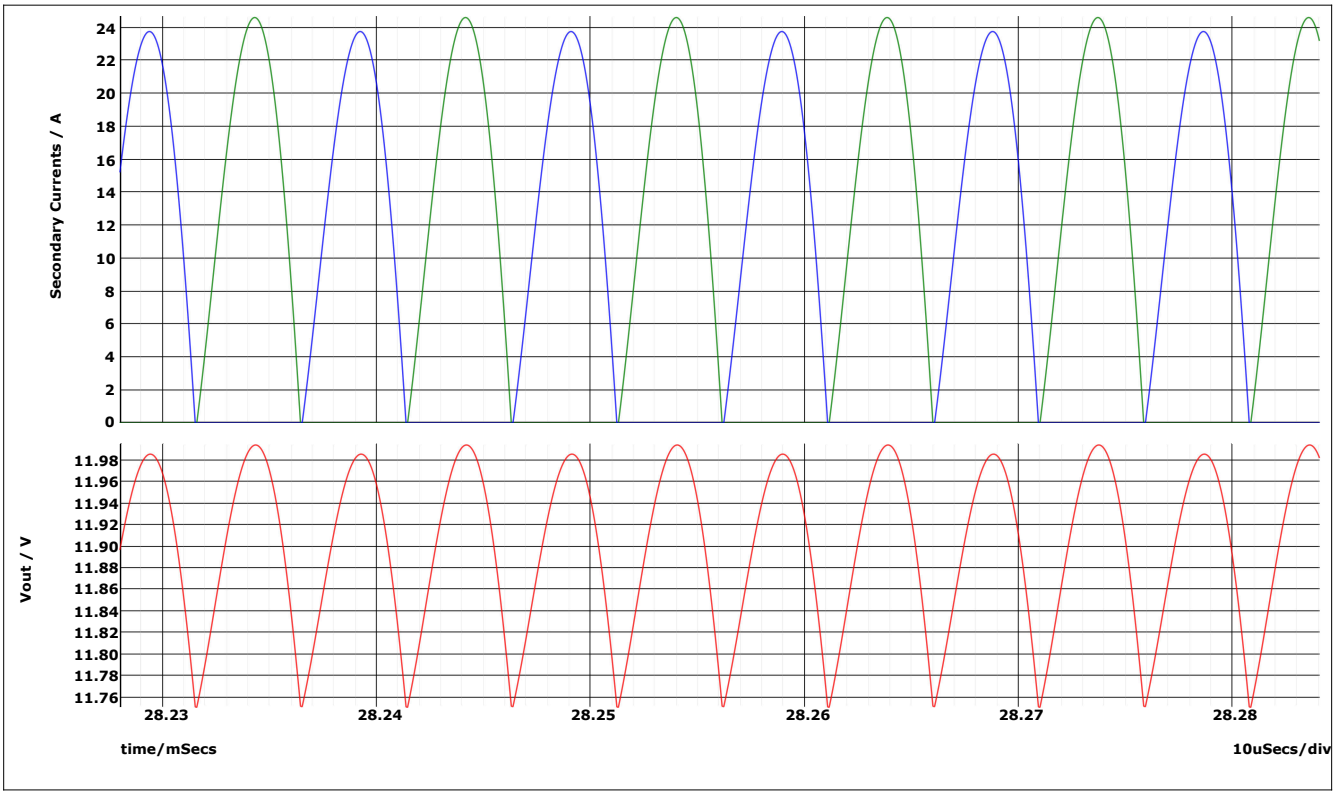


Figure 1-18. Case 2 Simulation results

1.12 How to design TL431 compensator for LLC with UCC25640x controller?

1.12.1 LLC Plant transfer Function under HHC Control

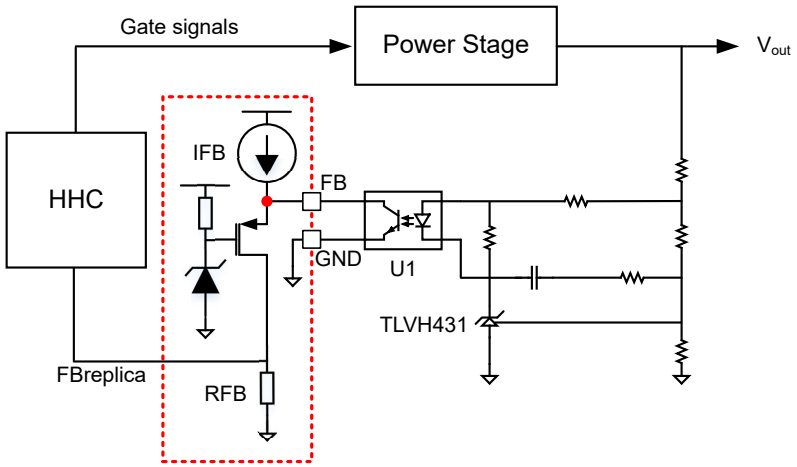


Figure 1-19. Feedback Chain Block Diagram

The reference [8] derives LLC plant transfer function$\left(\frac{V_{out}(s)}{FBreplica(s)}\right)$ when it is opearted under Hybrid Hysteretic Control. Simplis can also be used to extract the bode plots of the switching power converter. Here second method is followed.

UCC25640x EVM Power stage [3] is considered for extracting the gain plots when its operated under different input voltage and load conditions. In Figure 1-20, we can observe that plant gain plot is close to a single pole response in the low frequency region. So, Type 2 compensator (zero of the compensator should be located below low frequency pole of the plant) would be sufficient for secondary output voltage/current regulation. Here

low frequency pole is approximately located $f_p = \frac{1}{\pi R_L \cdot C_{out}}$ at where R_L is load resistance and C_{out} is output capacitance. If the cross over freqeuncy needs to be improved, then Type 3 compensator is recommended as at higher frequency regions plant transfer function has double poles which would degrade the phase [8].

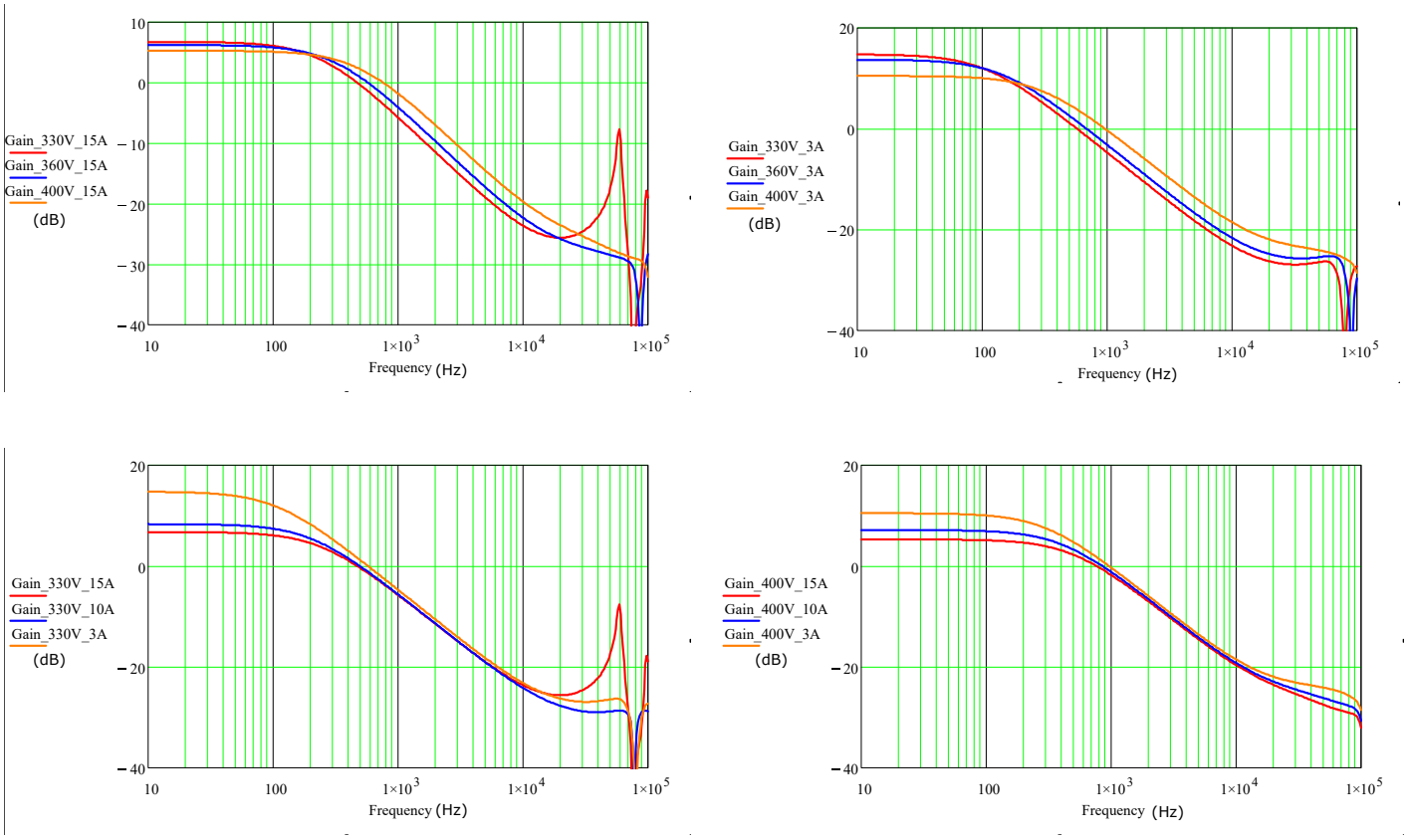


Figure 1-20. Gain plots under different input voltage and load conditions

1.12.2 Type 2 & Type 3 compensators with TL431:

1.12.2.1 Type 2 Compensator

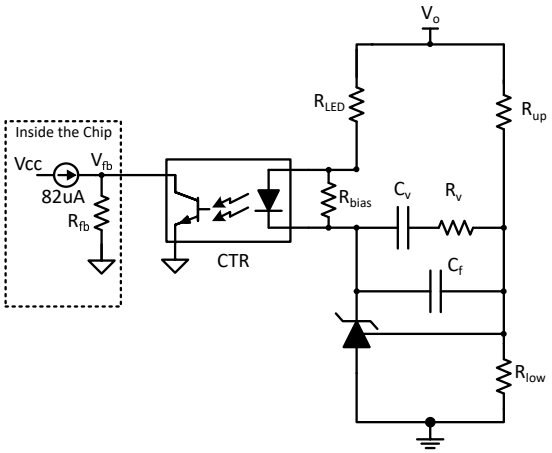


Figure 1-21. Type 2 compensator with fast lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{\left(C_v + C_f\right)\cdot R_{up}}\frac{1 + R_vC_vs}{\left(1 + \frac{sR_vC_vC_f}{C_v + C_f}\right)s} + 1\right) \quad (41)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v \cdot R_{up}}\frac{1 + R_vC_vs}{\left(1 + sR_vC_f\right)s} + 1\right) \quad (42)$$

$$\text{This can be written as } G_c(s) = G_o\left(\frac{\frac{\omega_L}{s} + 1}{1 + \frac{s}{\omega_{p1}}}\right) \quad (43)$$

$$\text{where } G_o = \frac{R_{fb}CTR}{R_{LED}}\left(1 + \frac{R_v}{R_{up}}\right) \quad \omega_L = \frac{1}{\left(R_v + R_{up}\right)\cdot C_v} \quad \omega_{p1} = \frac{1}{R_v \cdot C_f} \quad (44)$$

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole, CTR is current transfer ratio of opto coupler.

Note 1: During the full load to light load transition, the current through the opto coupler LED should be able to vary more than I_{fb}/CTR to regulate the output voltage. Here I_{fb} is maximum current provided by the FB pin. So, $R_{LED} \le \frac{V_o - V_{ref} - V_{LED}}{\left(I_{fb}/CTR\right)}$ where V_{ref} and V_{LED} are reference pin voltage and Opto coupler LED drop when its conducing.

Note 2: During startup, the entire output voltage will be applied across the shunt regulator as the shunt regulator starts sinking current only when reference pin voltage reaches the V_{ref} which corresponds to regulated output voltage. If this voltage exceeds the absoulte maximum cathode to anode voltage of the shunt regulator, it will be destroyed. In such scenarios, Type 2 compensator with out fast lane is recommended where zener diode is used in the fast lane which would clamp the voltage across the shunt regulator.

1.12.2.2 Type 2 compensator without Fast Lane

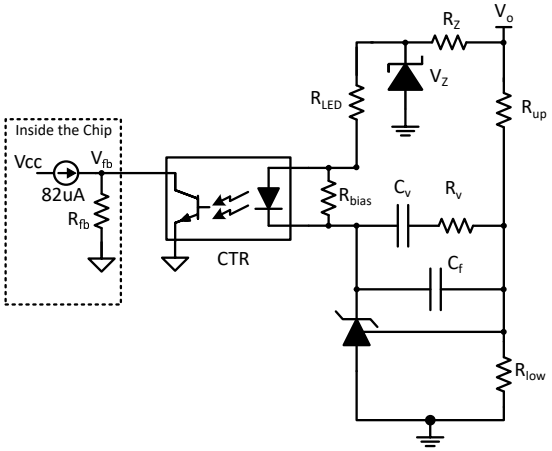


Figure 1-22. Type 2 compensator without fast lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{\left(C_v + C_f\right)\cdot R_{up}}\frac{1 + R_vC_vs}{\left(1 + \frac{sR_vC_vC_f}{C_v + C_f}\right)s}\right) \quad (45)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v \cdot R_{up}}\frac{1+R_vC_vs}{\left(1+sR_vC_f\right)s}\right) \quad (46)$$

$$\text{This can be written as } G_c(s) = G_o\left(\frac{\frac{\omega_L}{s}+1}{1+\frac{s}{\omega_{p1}}}\right) \quad (47)$$

$$\text{where } G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{R_v}{R_{up}}\right) \quad \omega_L = \frac{1}{R_v \cdot C_v} \quad \omega_{p1} = \frac{1}{R_v \cdot C_f} \quad (48)$$

Here ω_L is low frequency inverted zero and ω_{p1} is a high frequency pole.

1.12.2.3 Type 3 compensator with Fast Lane

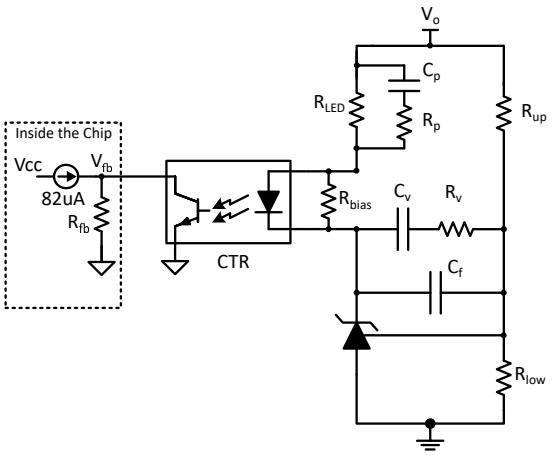


Figure 1-23. Type 3 compensator with fast lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = R_{fb}CTR\left(\frac{1}{\left(C_v+C_f\right)\cdot R_{up}}\frac{1+R_vC_vs}{\left(1+\frac{sR_vC_vC_f}{C_v+C_f}\right)s}+1\right)\left(\frac{1+sC_p\left(R_{LED}+R_p\right)}{R_{LED}\left(1+R_pC_ps\right)}\right) \quad (49)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{C_v \cdot R_{up}}\frac{1+R_vC_vs}{\left(1+sR_vC_f\right)s}+1\right)\left(\frac{1+sC_p\left(R_{LED}+R_p\right)}{1+R_pC_ps}\right) \quad (50)$$

$$\text{This can be written as } G_c(s) = G_o\left(\frac{\frac{\omega_L}{s}+1}{1+\frac{s}{\omega_{p1}}}\right)\left(\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_{p2}}}\right) \quad (51)$$

$$\text{where } G_o = \frac{R_{fb}CTR}{R_{LED}}\left(1+\frac{R_v}{R_{up}}\right) \quad \omega_L = \frac{1}{\left(R_v+R_{up}\right)\cdot C_v} \quad \omega_{p1} = \frac{1}{R_v \cdot C_f}$$
$$\omega_z = \frac{1}{\left(R_{LED}+R_p\right)\cdot C_p} \quad \omega_{p2} = \frac{1}{R_p \cdot C_p} \quad (52)$$

Here assuming $\omega_L \ll \omega_z \ll \omega_c \ll \omega_{p2} \ll \omega_{p1}$, ω_z and ω_{p2} creates the phase lead whereas ω_L implements the integrator to reduce the steady state error whereas ω_{p1} eliminates the effect of high frequency noise on the control loop. Here ω_c is cross over frequency.

1.12.2.4 Type 3 compensator without fast lane

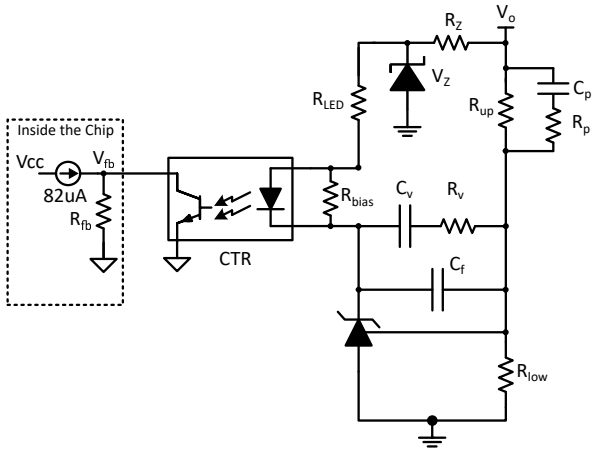


Figure 1-24. Type 3 compensator without fast lane

$$G_c(s) = \left|\frac{V_{fb}(s)}{V_o(s)}\right| = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{1}{(C_v + C_f)}\frac{1 + R_vC_vs}{\left(1 + \frac{sR_vC_vC_f}{C_v + C_f}\right)s}\right)\left(\frac{1 + sC_p(R_{up} + R_p)}{R_{up}(1 + R_pC_ps)}\right) \quad (53)$$

Assuming $C_f << C_v$, $G_c(s)$ further simplifies to

$$G_c(s) = \frac{R_{fb}CTR}{R_{LED}R_{up}}\left(\frac{1}{C_v}\frac{1 + R_vC_vs}{(1 + sR_vC_f)s}\right)\left(\frac{1 + sC_p(R_{up} + R_p)}{1 + R_pC_ps}\right) \quad (54)$$

$$\text{This can be written as } G_c(s) = G_o\left(\frac{\frac{\omega_L}{s} + 1}{1 + \frac{s}{\omega_{p1}}}\right)\left(\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_{p2}}}\right) \quad (55)$$

$$\text{where } G_o = \frac{R_{fb}CTR}{R_{LED}}\left(\frac{R_v}{R_{up}}\right) \quad \omega_L = \frac{1}{R_v \cdot C_v} \quad \omega_{p1} = \frac{1}{R_v \cdot C_f}$$
$$\omega_z = \frac{1}{(R_{up} + R_p) \cdot C_p} \quad \omega_{p2} = \frac{1}{R_p \cdot C_p} \quad (56)$$

Here assuming $\omega_L \ll \omega_z \ll \omega_c \ll \omega_{p2} \ll \omega_{p1}$, ω_z and ω_{p2} creates the phase lead whereas ω_L implements the integrator to reduce the steady state error whereas ω_{p1} eliminates the effect of high frequency noise on the control loop. Here ω_c is cross over frequency.

1.12.3 Type 3 Compensator Design Example

The power stage of the UCC25640x EVM [3] is considered to demonstrate the Type 3 compensator design which is shown in Figure 1-25 [1.12.2.3]. Lets consider 10kHz as a cross over frequency (f_c) for the loop gain.

1. From Figure 1-20, the open loop gain $\left(G_{plant}(s) = \frac{V_{out}(s)}{FBreplica(s)}\right)$ is close to -25dB at 10kHz.
2. So $G_c(s)$ should be 25dB at the cross over frequency.
3. Assuming $f_L \ll f_z \ll f_c \ll f_{p2} \ll f_{p1}$ in [1.12.2.3], $G_c(s)$ is approximated as $G_o \cdot \frac{f_c}{f_z}$. For a given phase lead (θ), cross over frequency (f_c), f_z, f_{p2} can be found out using following equations [9]: $f_c = \sqrt{f_z \cdot f_{p2}}$, $f_z = f_c\sqrt{\frac{1 - \sin(\theta)}{1 + \sin(\theta)}}$, $f_{p2} = f_c\sqrt{\frac{1 + \sin(\theta)}{1 - \sin(\theta)}}$. So, $G_c(s) \cong G_o \cdot \frac{f_c}{f_z} = G_o \cdot \frac{\sqrt{f_z \cdot f_{p2}}}{f_z} = G_o \cdot \sqrt{\frac{f_{p2}}{f_z}}$.
4. For a phase lead of 52°, f_z and f_{p2} should be 3.4kHz and 29kHz respectively.

5. Since f_z,f_{p2} are found out, G_o can be obtained using following expression: $G_o \cdot \sqrt{\frac{f_{p2}}{f_z}} = 17.78 \Rightarrow G_o = 6.126$ (25dB=17.78).
6. f_{p1} is a high frequency pole which is used to eliminate the high frequency noise. It is recommened to place this pole close to ESR of the output capacitor. Here f_{p1} is chosen as 479kHz.
7. f_L should be chosen such that controller should be able to regulate the output voltage when the converter operates in the burst mode. So, f_L should be less than the burst mode frequency. In this design, f_L is considered as 88Hz.
8. Rup and Rlow can be found out using following expressions: $\frac{V_o - V_{ref}}{R_{up}} = I_{ref} + \frac{V_{ref}}{R_{low}}$ where V_o is output voltage and V_{ref}, I_{ref} are reference voltage and bias current through the reference pin of the shunt regulator. To make V_o independent of the I_{ref}, the I_{ref} should be much lower than $\frac{V_o - V_{ref}}{R_{up}}$. So, $\frac{V_o - V_{ref}}{R_{up}} = \frac{V_{ref}}{R_{low}}$. In the EVM, TLVH431 is considered for which reference voltage is given as 1.24V. For this design, $\frac{V_o - V_{ref}}{R_{up}}$ is considered as 73uA. So R_{up} obtained as 147kOhm. And from $\frac{V_o - V_{ref}}{R_{up}} = \frac{V_{ref}}{R_{low}}$, R_{low} obtained as 16.98kohm.
9. Consider C_f as 10pF. So, R_v can be obtanied as
   $\omega_{p1} = \frac{1}{R_v \cdot C_f} \Rightarrow f_{p1} = \frac{1}{2 \cdot \pi \cdot R_v \cdot C_f} \Rightarrow R_v = \frac{1}{2 \cdot \pi \cdot 479kHz \cdot C_f} \Rightarrow R_v = 33.2kohm$
10. R_{LED} can be obtanied as
    $G_o = \frac{R_{fb} CTR}{R_{LED}}\left(1 + \frac{R_v}{R_{up}}\right) \Rightarrow R_{LED} = \frac{R_{fb} CTR}{G_o}\left(1 + \frac{R_v}{R_{up}}\right) \Rightarrow R_{LED} = \frac{100 \cdot 10^3 \cdot 0.2}{6.126}\left(1 + \frac{33.2k}{147k}\right) \Rightarrow R_{LED} = 4kohm$
11. C_v can be obtanied as
    $\omega_L = \frac{1}{(R_v + R_{up}) \cdot C_v} \Rightarrow C_v = \frac{1}{2 \cdot \pi \cdot f_L \cdot (R_v + R_{up})} \Rightarrow C_v = \frac{1}{2 \cdot \pi \cdot 88 \cdot (33.2k + 147k)} \Rightarrow C_v = 10nF$
12. C_p, R_p are obtanied as
    $\omega_z = \frac{1}{(R_{LED} + R_p) \cdot C_p}$, $\omega_{p2} = \frac{1}{R_p \cdot C_p} \Rightarrow f_z = \frac{1}{2 \cdot \pi \cdot (R_{LED} + R_p) \cdot C_p}$, $f_{p2} = \frac{1}{2 \cdot \pi \cdot R_p \cdot C_p}$
    $\Rightarrow 3.4kHz = \frac{1}{2 \cdot \pi \cdot (R_{LED} + R_p) \cdot C_p}$, $29\text{kHz} = \frac{1}{2 \cdot \pi \cdot R_p \cdot C_p} \Rightarrow C_p = 10nF$, $R_p = 540ohm$.
13. Rbias is used to bias the shunt regulator. R_{bias} is obtained as $R_{bias} = \frac{V_{opto}}{I_{bias}} = \frac{1V}{1mA} = 1kohm.$

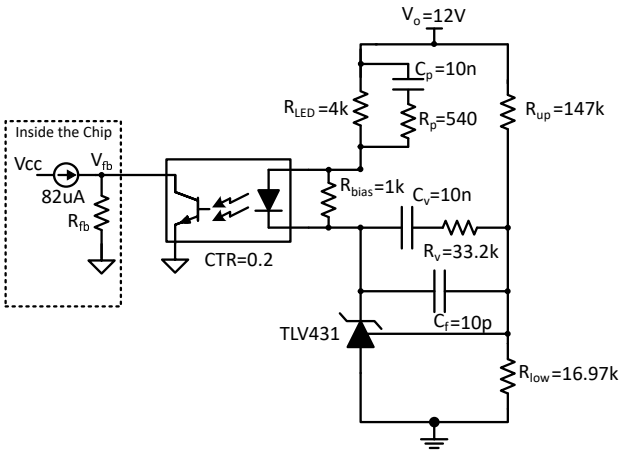


Figure 1-25. Type 3 compensator

2 References

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4. *Wurth Transformer datsheet*
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