UC1525AJ

Device Design Question Consultation

Dear TI Technical Engineer，

Thank you very much for your attention and answers to our questions, your help in analyzing our questions is very important. In response to some of your questions before, I will explain again here to help you better help us analyze.

NOTE：Figure 1 is an example of the application of UC1525AJ chip by our company.

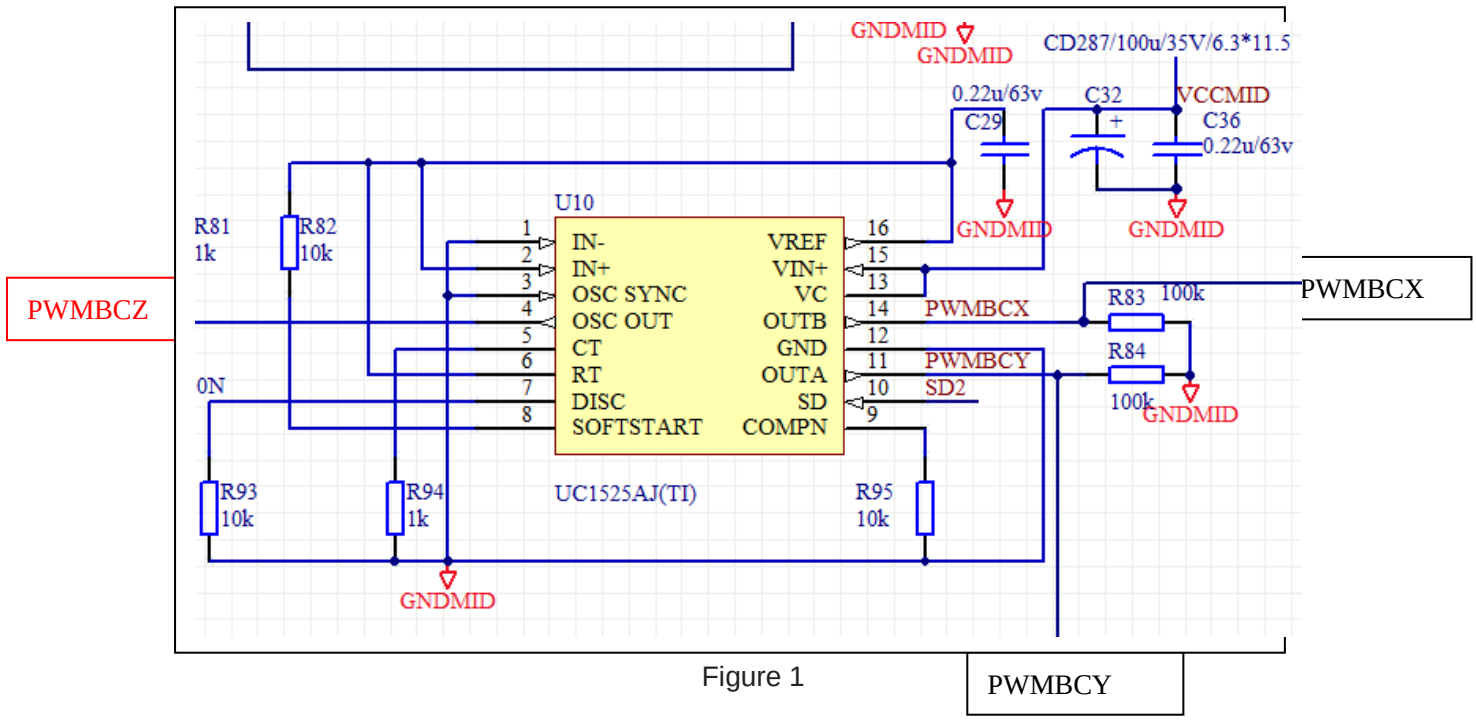
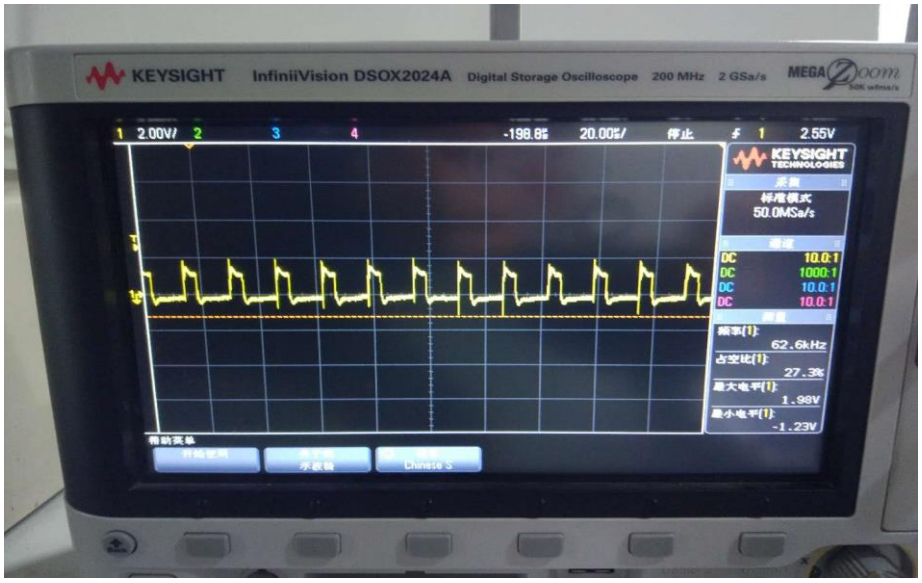


Figure 1

At this stage, the main reason why we consulted you about this UC1525AJ device is that the IGBT and the voltage regulator on the driver board often burst during the operation of our products. In view of this, we have investigated the application of this device on our current schematic. Is the rationality of the peripheral device design for this device reasonable? I hope to get your assessment, is there any unreasonable device selection? If not, how to improve? I hope to get your guidance and analysis.

NOTE：1、How to control the parameters of the two pins of OSC SYNC and OSC OUT? How much control can you guarantee that this UC1525AJ is working properly?

2、Regarding the UC1525AJ device, how do you think Zhou Wei is the most reasonable? Is there a circuit design that can be recommended for this UC1525AJ device?



5th foot on the 2st foot test waveform