UCC21225A SCH Review and PCB Recommendations

Disclaimer

The information provided on this page represents TI's knowledge and belief as of the date that it is provided. No guarantees as to device or system performance are implied.

Rev	Date released	Changes	Author
1.0	-	Initial release	(Author name)

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TI Comments
(TI summary of findings in the review)

Glossary

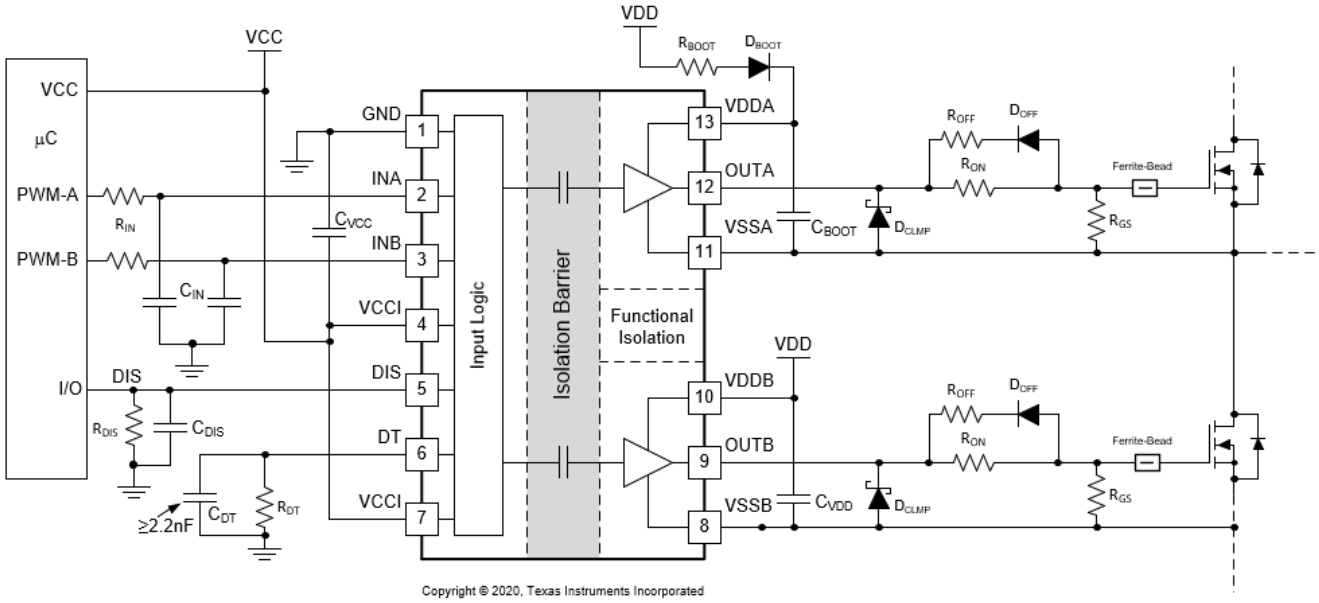
For each component:

- A component labeled REQUIRED denotes it is necessary for normal operation of the driver and may have significant consequences if omitted.
- A component labeled RECOMMENDED denotes that TI thinks its usage provides system benefit and recommends its usage to achieve best device performance.
- A component labeled OPTIONAL denotes that its usage depends on a specific configuration and may provide benefits in a limited scope.

When TI checks the schematic:

- An evaluation of GOOD means that TI thinks the components/circuit connected to a pin and usage of the pin are acceptable and will allow normal system function
- An evaluation of NEEDS REVIEW means that TI sees an issue with the components/circuit connected to a pin or usage of the pin. Schematic review checklist table below is expected to be followed.
- An evaluation of NOT APPLICABLE means that the design doesn't use configure or enable a specific features.

Typical Device Schematic



Primary-side Checklist

System	Pin #	PIN Name	Component Name	Usage is?	Component Function	Typ. Value	Component Details	Layout Suggestions	Evaluation	Comments
Bypass Caps	**4,7**	**VCCI**	C_{VCCI}	REQUIRED	Big Decoupling Cap	>1uF	Tantalum or Electrolytic parallel to small capacitor when when bias supply is a at a relatively long distance from VCCI	Place on same side 5mm away from the pin. Prioritize the placement of the smaller cap closer to the driver.	GOOD	
				REQUIRED	Small Decoupling Cap	>100nF	25V , MLCC, X7R recommended			
Input Signal	**2,3**	**INA** **INB**	R_{IN}	REQUIRED	Input RC Filter	0 - 100	Helps to filter out ringing induced by non-ideal layout or long PCB traces	Place on same side 5mm away from the pin.	NEEDS REVIEW	
			C_{IN}	REQUIRED		10pF - 100pF				
Programable Dead Time	**6**	**DT**	R_{DT}	REQUIRED	User Defined Dead Time	Based on DT equation RDT in k 500 - 500k $t_{DT}(ns) = 10 \times R_{DT}(k\Omega)$	For larger values of DT, it is recommended placing a ceramic capacitor for higher noise immunity	Place on same side 5mm away from the pin.	NEEDS REVIEW	
			C_{DT}	REQUIRED	Helps Noise Immunity	>2.2nF				
Disable	**5**	**DIS**	R_{DIS}	REQUIRED	Pull Down Resistor	10k	Recommended to use a capacitor of low ESR/ESL close to DIS pin when connecting to a microcontroller with distance	Place on same side 5mm away from the pin.	GOOD	
			C_{DIS}	REQUIRED	Helps Noise Immunity	1nF				

Secondary-side Checklist

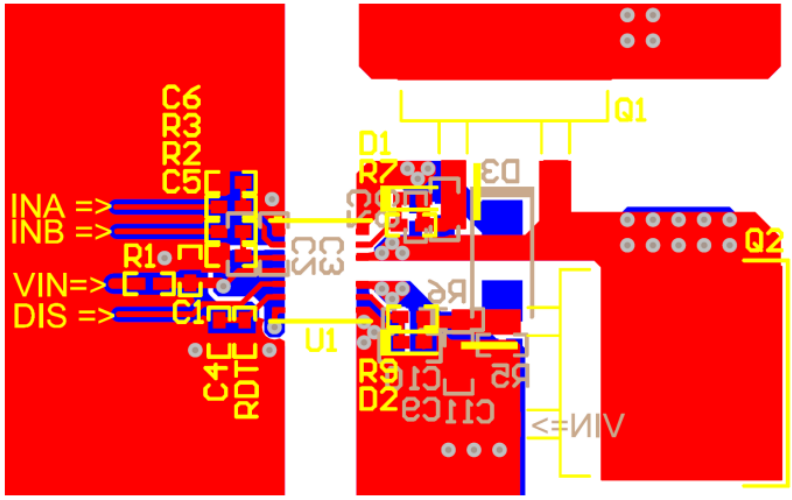
System	Pin #	PIN Name	Component Name	Usage is?	Component Function	Typ. Value	Component Details	Layout Suggestions	Evaluation	Comments
Gate Drive	11,12 8,9	OUTX VSSX	R_{ON}	REQUIRED	External Turn ON Resistor	Design based on specifications $I_{OA+} = MIN(4A, \frac{V_{DD}-V_{BDF}}{R_{NMOS}\|\|R_{OH}+R_{ON}+R_{GFET-Int}})$	It is recommended to have placeholders to allow for different gate drive strength when turning ON /OFF the power switches.	Place capacitor on the same side 5mm away from the pin. High priority layout. Place gate resistors as close to the gate as possible.	NEEDS REVIEW	
			R_{OFF}	OPTIONAL	External Turn OFF Resistor	Design based on specifications $I_{OA+} = MIN(6A, \frac{V_{DD}-V_{BDF}-V_{GDF}}{R_{OL}+R_{OFF}\|\|R_{ON}+R_{GFET-Int}})$				
			D_{OFF}	OPTIONAL	Anti-parallel Diode					
			R_{GS}	OPTIONAL	Pull Down Resistor	5.1k - 20k	Mitigates risk of dv /dt induced turn-on due to miller current	Place as close to the gate as possible.	NEEDS REVIEW	
			Ferrite-Bead	OPTIONAL	Reducing Gate Ringing	Low resistance value during normal operation	Example Part number: MPZ1608S101A It's recommended to have placeholders for this component in a high power, fast switching application.			
			D_{CLMP}	OPTIONAL	Driver Output Clamp	Schottky	It's recommended to have placeholders for this component in a high power, fast switching application	Clamp diode should be place close to the driver pin.	NEEDS REVIEW	
Bootstrap	11,13	VDDA VSSA	C_{BOOT}	REQUIRED	Bootstrap Capacitor	Based on design specifications $C_{BOOT} = \frac{Q_{TOTAL}}{\triangle V_{VDDA}}$	Use the calculator for the design of the Bootstrap	Bootstrap capacitor and bypass capacitor should be place as close as possible to the gate driver supply pins Minimize high current path that includes CBOOT, DBOOT, and RBOOT. This will minimize parasitic inductances and reduce high current trace lengths.	NEEDS REVIEW	
			R_{BOOT}	REQUIRED	Bootstrap Resistor	1 - 20 $I_{DBoot(pk)} = \frac{V_{DD}-V_{BDF}}{R_{Boot}}$	Depending on the diode used. Use to reduce the inrush current in DBOOT and limit the ramp up slew rate voltage of VDDA-VSSA during each switching cycle.			
			D_{BOOT}	REQUIRED	Bootstrap Diode	High Voltage(Voltage rating should be higher than the DC link), fast recovery diode or SiC Schottky diode with a low forward drop voltage and low junction capacitance				

VDDB Capacitor	**8,10**	**VDDB** **VSSB**	C_{VDD}	REQUIRED		10uF parallel with 220nF	50V , MLCC, X7R recommended	Place as close as possible to the gate driver supply pins.	NEEDS REVIEW	
						10uF	Tantalum or Electrolytic			

UCC21225 Unused pins

Side	Pin Name	Pin #s	What to do if Unused	Urgency
Primary	INA or INB	2 or 3	Tie to ground for better noise immunity	REQUIRED
	DIS	5	Tie to ground for better noise immunity	REQUIRED
	DT	6	If Dead Time is no required and overlapping the outputs is allowed, DT pin can be connected to VCCI to disable Dead Time feature. It is not recommended to leave DT floating since external noise can couple into the pin affecting the outputs behavior.	REQUIRED

UCC21225 Layout Recommendations



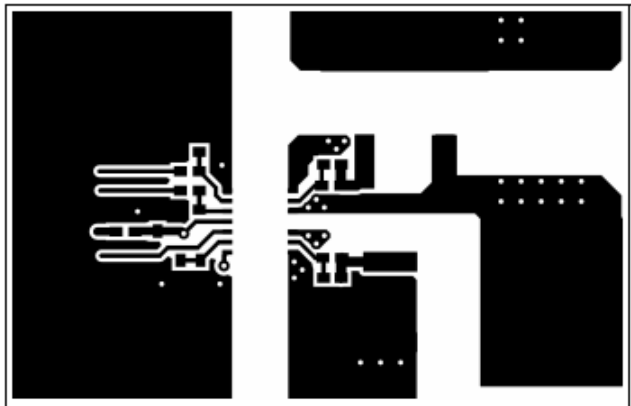


Figure 42. Top Layer Traces and Copper

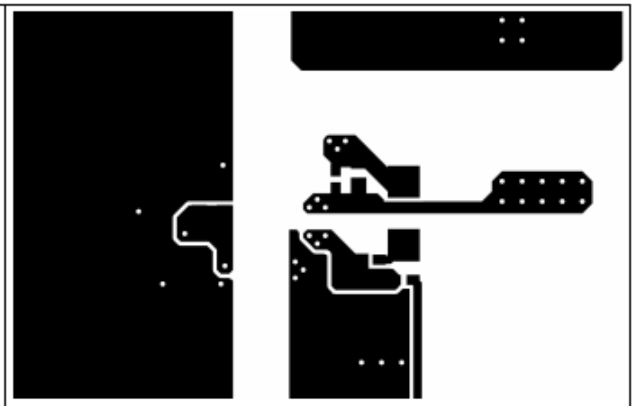


Figure 43. Bottom Layer Traces and Copper

	Recommendations	Urgency	Comments

Component Placement	• Decoupling capacitors should be placed as close as possible to the device pins • Minimize parasitic inductance between HS source transistor and LS source transistor to avoid large negative transient currents	REQUIRED	
Grounding Considerations	• Driver should be place as close as possible to the transistors. Minimize loop inductance and noise in gate terminals by confining the high peak currents that charge and discharged transistor gates • Minimize loop design for the bootstrap circuit.	REQUIRED	
High Voltage Considerations	• To ensure isolation performance between primary and secondary side, avoid placing any PCB traces or copper below the driver device. PCB cutout is recommended to increase the creepage • For half-bridge or high-side/low-side configurations, maximize the clearance distance of the PCB layout between the high and low-side PCB traces.	REQUIRED	
Thermal Considerations	• If there are multiple layers in the system, it is also recommended to connect the VDDA, VDDB, VSSA and VSSB pins to internal ground or power planes through multiple vias of adequate size. Ensure that no traces or copper from different high-voltage planes overlap. • Increasing the PCB copper connecting to VDDA, VDDB, VSSA and VSSB pins is recommended, with priority on maximizing the connection to VSSA and VSSB. However, high voltage PCB considerations mentioned above must be maintained.	REQUIRED	