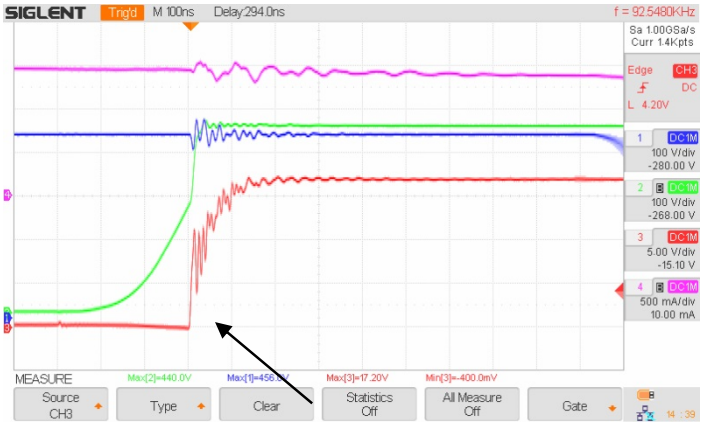

Fig 1) UCC21520 - Typical High Side Gate Turn on (Gate A)

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Transition)

CH3) V_{GS}[Q7] ,GATE A Turn on (Measured W/ Isolated Probe)

CH4) Shim Inductor Current in Full Bridge

The Gate Drive Turn on is well behaved with little to no overshoot. The corresponding Drain Transition is also well Behaved

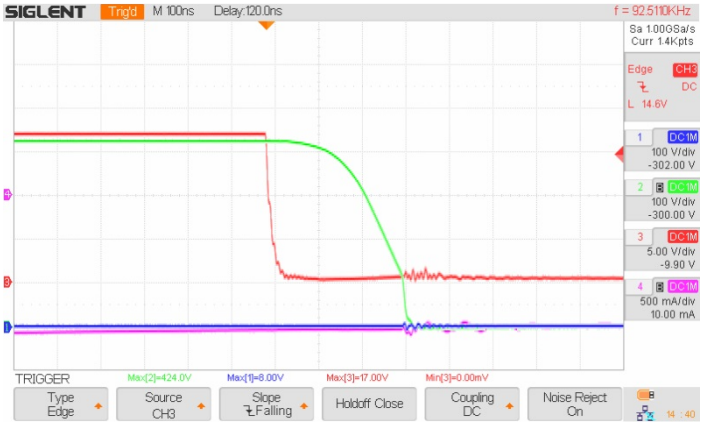

Fig 1) UCC21520 - Typical High Side Gate Turn off (Gate A)

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Transition)

CH3) V_{GS}[Q7] ,GATE A Turn off (Measured W/ Isolated Probe)

CH4) Shim Inductor Current in Full Bridge

The Gate Drive Turn off is also well behaved with little to no overshoot. The corresponding Drain Transition is also well Behaved

Fig 3) Typical Continuous operation of the Gate Driver

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Driver)

CH3) Boot Strap Cap (Measured W/ Isolated Probe)

The .1uF Bootstrap Cap charges quickly (within 200ns), and discharges approximately 0.8V to provide the necessary Qg to the upper MOSFET.

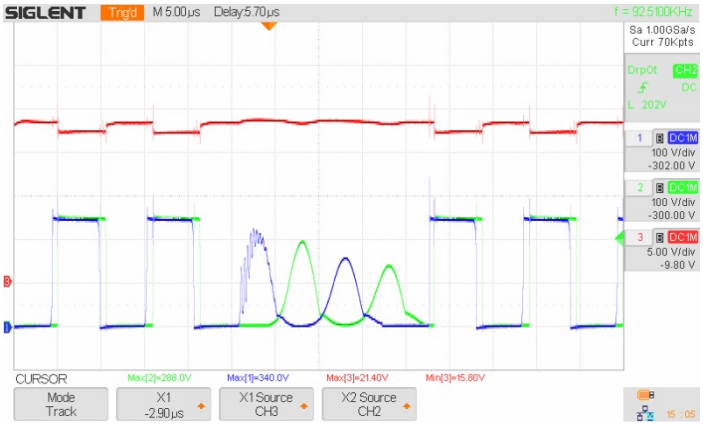

Fig 3) Entering Cycle Skip Mode at Very Light Loads

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Driver)

CH3) Boot Strap Cap (Measured W/ Isolated Probe)

The .1uF Bootstrap Cap charges quickly (within 200ns), and refreshes several times during the ring down oscillation of the Bridge. No abnormally high Voltages are seen, even with noise Max is 21.4V. The actual Maximum Bootstrap Voltage is Approximately 18.4V.

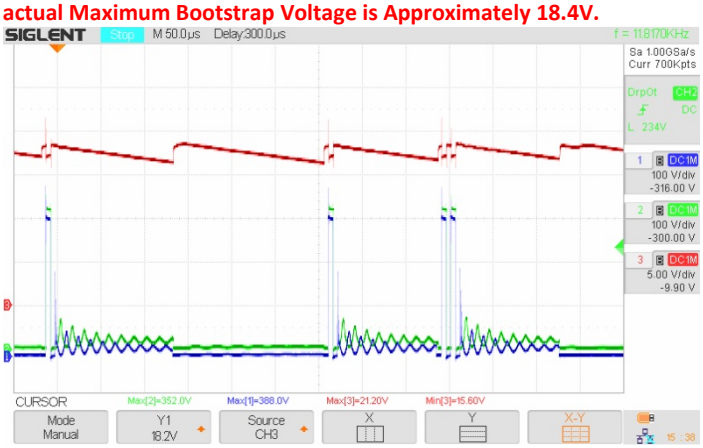

Fig 5) Very Deep into Burst Mode during No-load Operation.

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Driver)

CH3) Boot Strap Cap (Measured W/ Isolated Probe)

The .1uF Bootstrap Cap discharges significantly between pulses, but recharges quickly, correctly, and without overshoot.

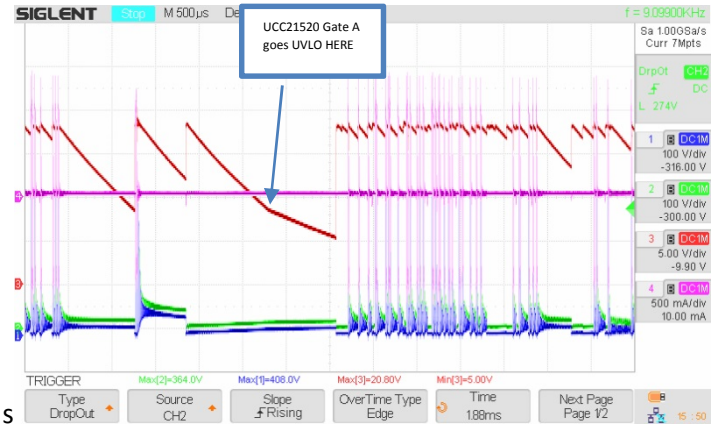

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Fig 6) Very Deep into Burst Mode – Showing a UVLO and Recovery.

CH1) Source C (One Leg of Full Bridge)

CH2) Source A (The Full Bridge Leg Corresponding to this Driver)

CH3) Boot Strap Cap (Measured W/ Isolated Probe)

At random, a gap inpulses long enough to cause UVLO is encountered. Even after this, the driver refreshes the bootstrap cap without issue or observed anomaly. We see nothing that violates datasheet conditions

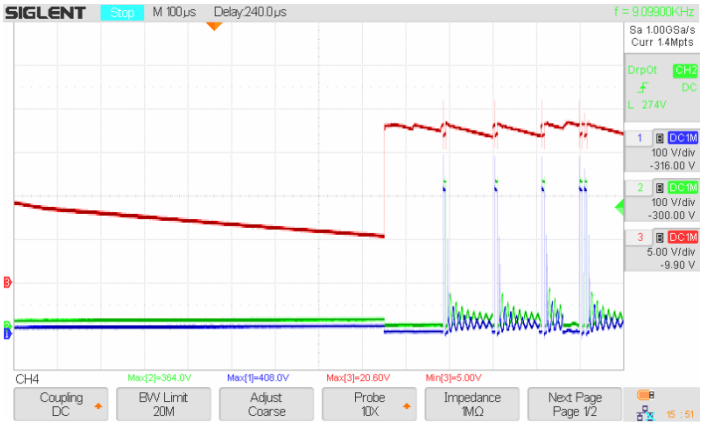


Fig 7) Very Deep into Burst Mode – Showing a UVLO and Recovery.

CH1) Source C (One Leg of Full Bridge)

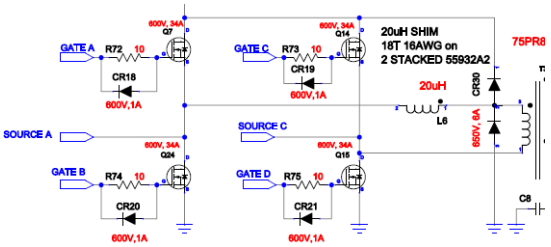
CH2) Source A (The Full Bridge Leg Corresponding to this Driver)

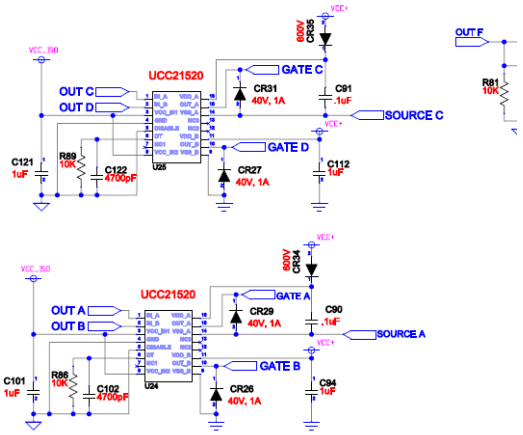
CH3) Boot Strap Cap (Measured W/ Isolated Probe)

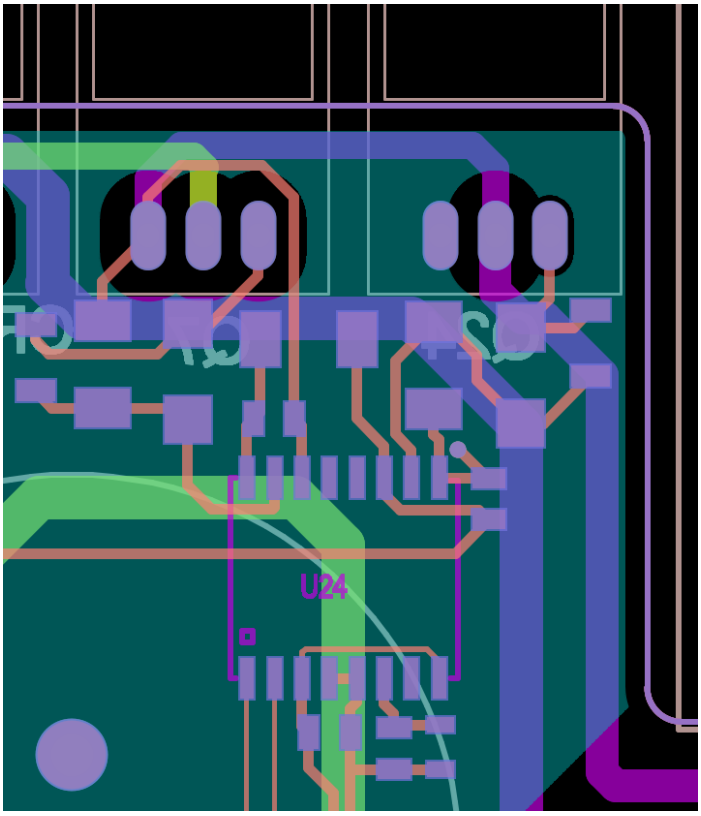
This is a zoom of Figure 6. Note the clean turn on behavior of the Bootstrap cap. Note the very High dv/dt of the bootstrap refresh.

Schematic and layouts are shown below

This pair of UCC21520 is used with UCC28950 ZVS Full Bridge Controller







EXAMPLE LAYOUT OF UCC21520 SECTION

2ND DRIVER IS LAID OUT IDENTICALLY

GENERAL NOTES:

- **THERE IS APPRECIABLE (~1Vpp) RIPPLE ON THE 0.1Uf BOOSTRAP CAP DUE TO CHARING OF Qg. This is not of concern to us, as any voltage of UVLO is sufficient for our gate drive requirements**
- **The bootstrap cap is 0.1uF, locally charged through an ultrafast diode from a 1.0uF Ceramic Cap. There is no resistance in the charging path in order to ensure a quick refresh of the voltage**
  - **The capacitors *could* be increased, but we still would like to know what conditions, If any, are being violated right now.**
  - **The dv/dt of bootstrap recharging is very fast**
- **During load dumps and transitions, UCC21520 will occasionally go into UVLO, but comes out of it normally when switching resumes**
  - **This alone is not concerning to us**
- **Failures of UCC21520 always occur after repeated load dumps when the converter will temporarily go into deep burst mode, or temporarily suspend switching.**
- **The layout is very tight. Gate drives are clamped from negative transients by schottky diodes**

Questions

- **Are there unpublished limitations on allowable dv/dt of VDDA/ VDDB that might occur on bootstrap recharging**
- **Is there an unpublished transient immunity dv/dt limitation with respect to VDDA vs VDDB??**
  - **Only CMTI limitations for Primary to secondaries is published**