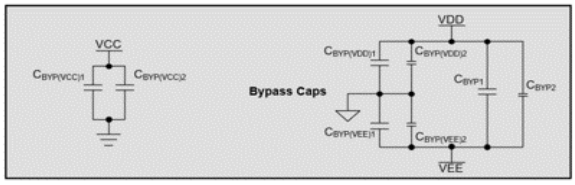
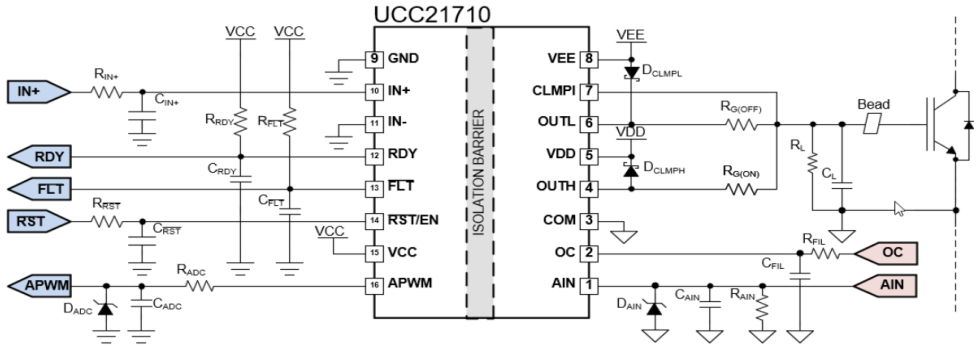
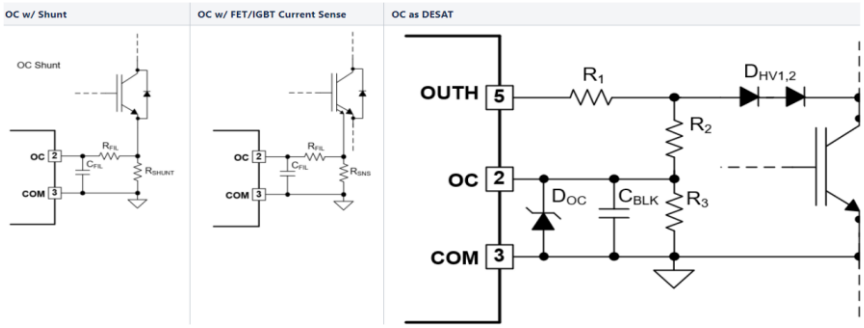






TI's best practice recommendations

System	Pin #	PIN Name	Component Name	Usage is?	Component Function	Typ. Value	Component Details	Layout Suggestions
PRIMARY SIDE								
Analog-to- PWM Channel	16	APWM	R_{ADC}	Optional	LPF converts PWM to analog signal	20kΩ	LPF is **NOT** used if the controller is taking the duty cycle and converting it to voltage in software X7R type	Place RC filter close to ADC/MCU input
			C_{ADC}	Optional		2200pF		
Bypass Caps	15	VCC	$C_{BYP(VCC)1}$	Required	High Value Decoupling Cap	100nF-1µF	X7R recommended	Place on same side ≤2mm away from the pin.
			$C_{BYP(VCC)2}$	Required	Low value Decoupling Cap	1nF-100nF		Prioritize the placement of the smaller cap closer to the driver.
Fault Reset	14	RST/EN	R_{RST}	Recommended	Input RC filter	100Ω		Place capacitor on the same side ≤2mm away from the pin
			C_{RST}	Recommended		100pF	X7R recommended	
Fault Signal	13	FLT	R_{FLT}	Required	Pullup Resistor	5.1k		Place capacitor on the same side ≤2mm away from the pin
			C_{FLT}	Recommended	Filter cap	100pF	X7R recommended	
Power-Good Signal	12	RDY	R_{RDY}	Required	Pullup Resistor	5.1k		Place capacitor on the same side ≤2mm away from the pin
			C_{RDY}	Recommended	Filter cap	100pF	X7R recommended	
PWM Input	11, 10	IN+, IN-	R_{IN+}	Recommended	Input RC Filter	100Ω	IN- is usually grounded unless differential signalling or interlock is used	Place capacitor on the same side ≤2mm away from the pin
			CIN+	Recommended		100pF		

IGBT/FET	n/a	Gate	R_L	Optional	Gate pull down resistor	10kΩ		Place as close to gate as possible. It's recommended to have placeholders for this component in a high power, fast switching application during a prototype build to enable testing if necessary
			C_L	Optional	Capacitor to slow down gate dV/dt	1nF-100nF	50V rated, X7R recommended	
			Ferrite Bead	Recommended	Reduce gate ringing	Low resistance value during normal operation	Example Part number: MPZ1608S101A	
Bypass Caps	8	VDD	$C_{BYP(VDD)1}$	Required	High Value VDD-COM Decoupling Cap	1µF-10µF	50V rated, X7R recommended	Place capacitor on the same side ≤2mm away from the pin. Prioritize the placement of the smaller value caps (..2) closest to the driver. It's recommended to have placeholders for these components in a high power, fast switching application during a prototype build to enable testing if necessary.
			$C_{BYP(VDD)2}$	Required	Low Value VDD-COM Decoupling Cap	100nF-220nF		
	5	VEE	$C_{BYP(VEE)1}$	Required	High Value VEE-COM Decoupling Cap	1µF-10µF	50V rated, X7R recommended	
			$C_{BYP(VEE)2}$	Required	Low Value VEE-COM Decoupling Cap	100nF-220nF		
			C_{BYP1}	Recommended	High Value VDD-VEE Decoupling Cap	1µF-10µF	50V rated, X7R recommended	
			C_{BYP2}	Recommended	Low Value VDD-VEE Decoupling Cap	100nF-220nF		
Miller Clamp	7	CLMPI	NA	Required				Keep the connection trace shorter between CLMPI pin to GATE
Gate Drive	6	OUTL	$R_{G(OFF)}$	Required	Gate pull-down resistance	2Ω-10Ω	Can be several parallel resistors	Highest priority layout (along with decoupling caps), Gate resistor should be placed close to gate as possible.
			D_{CLMPL}	Optional	Driver Output clamp	Schottky		Clamp diode close to driver pin.
	4	OUTH	$R_{G(ON)}$	Required	Gate pull-up resistance	2Ω-10Ω	Can be several parallel resistors	It's recommended to have placeholders for these components in a high power, fast switching application during a prototype build to enable testing if necessary.
			D_{CLMPH}	Optional	Driver Output clamp	Schottky		
APWM Input Conditioning	1	AIN	C_{AIN}	Optional	Filtering Cap	100pF-10nF	X7R recommended	Place close to device pins
			R_{AIN}	Optional	I-V conversion	5kΩ		
			D_{AIN}	Optional	OV protection		–5V Zener	
OC w/ Shunt	2	OC	R_{FIL}	Recommended	RC Filter	100Ω-1kΩ		Place Close to Device
			C_{FIL}	Recommended		100pF-1nF	X7R recommended The delay from the RC filter should be considered in the overall short-circuit/over-current detection time.	
			R_{SHUNT}	Required	Conversion	Value selected based on Peak collector current		Sensitive signal routing
OC w/ SenseFET			R_{FIL}	Recommended	RC Filter	100Ω-1kΩ		Place Close to Device
			C_{FIL}	Recommended		100pF-1nF	X7R recommended The delay from the RC filter should be considered in the overall short-	
			R_{SNS}	Required	Sense Current I-V Conversion	Value selected based on Peak collector current		Sensitive signal routing
OC as DESAT			$R_{1,2,3}$	Required	Current source generation	See UCC217xx XL Calculator		Sensitive signal routing
			C_{BLK}	Required	Blanking capacitor			Place close to device
			$D_{HV1,2}$	Required	HV Block Diodes			Sensitive signal routing
			D_{OC}	Recommended	OV Protection			Sensitive signal routing

UCC217xx Calculator: OC (Over-Current)

How to use this calculator:
1) Input system information in User Input (parameter descriptions are shown under Definitions).
2) Driver parameters from the datasheet are given in the Fixed Value section.
3) See Calculator Output for OC calculations based on the System and Driver Parameter values.

Note: OC configuration is only available with UCC21732 and UCC21710.

User Inputs

System Parameters						
VDD	R1 (Ω)	R2 (Ω)	R3 (Ω)	Vfw (V)	n	CBLK (nF)
15	15000	9100	2000	1.4	1	1

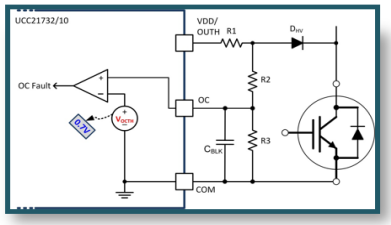
Fixed Value

Driver Parameters
VOCTH (V)
0.7

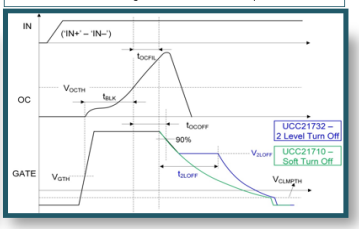
Calculator Output

VOCDET (V)	tBLK (ns)
2.49	1734.18

Parameter	Definition
VDD	Positive drive voltage
RDESAT	Resistor in series with HV blocking diode to limit current
R1	Resistor to set blanking capacitor charge current
R2	Part of resistor divider to control DESAT threshold voltage
R3	Part of resistor divider to control DESAT threshold voltage
Vfw	Forward voltage drop across HV blocking diode
n	Number of HV blocking diodes in series
CBLK	Capacitor to set blanking time (C1 in equation)
VOCTH	Internal OC detection threshold voltage
VOCDET	Actual detection voltage considering all external components
tBLK	Blanking time before DESAT detection



OC Timing Diagram (OC is the voltage at the OC pin and GATE is the voltage at the IGBT/MOSFET)



$$V_{OCDET} = V_{OCTH} * \frac{R2 + R3}{R3} - n * V_F$$

$$t_{BLK} = -\frac{R1 + R2}{R1 + R2 + R3} * R3 * C1 * \ln\left(1 - \frac{R1 + R2 + R3}{R3} * \frac{V_{OCTH}}{VDD}\right)$$