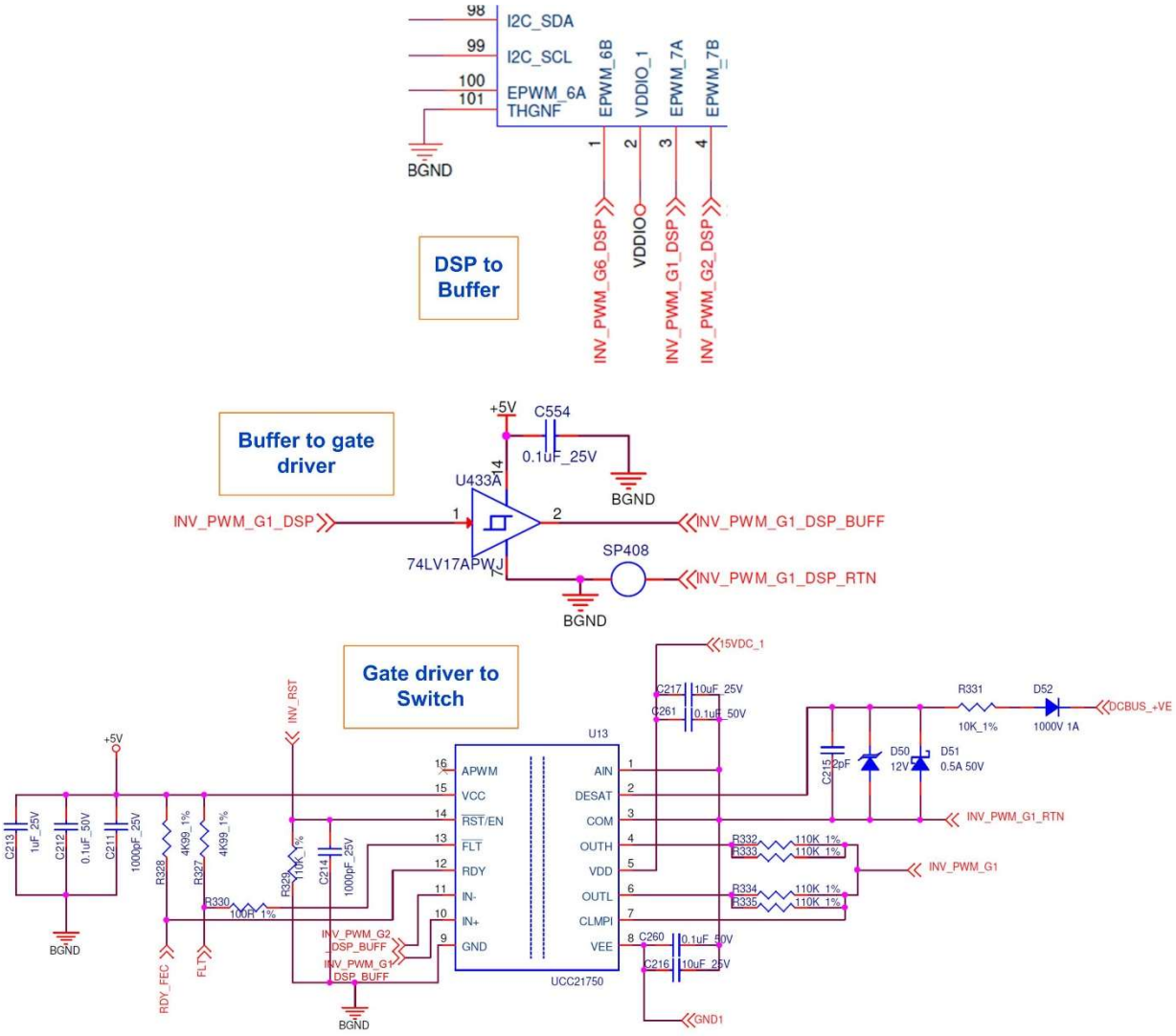
UCC21750 Schematic Review:



Suggestions:

1. Consider adding ESD diode at AIN for OV protection (optional)
2. Increase the DESAT pin bypass capacitor (C215) to at least 220pF (make sure this and all bypass caps are close to device pins)
3. The resistances on the OUTL/OUTH pins are very large, this will cause increased switching loss and decreased peak sink/source current. Unless you are trying to slow down the switching speed of the FET these resistances don't need to be so large.
4. Make sure that the trace between the CLMPI pin and the gate is short
5. Consider an input RC filter at the IN+/IN- pins (optional)
6. Like FLT pin, RDY pin should have 5.1k pull up

7. R329 should be in series with C214 to create input filter, not in parallel