1-Answer to Question 1

We have observed the HO/LO waveforms (TR3 and TR5 gates) of U2 (UCC256403), so please check the waveforms in 1-1 and 1-2 below.

1-1. Measurement of TR3 and TR5 gate voltages in steady state

<Measurement conditions>

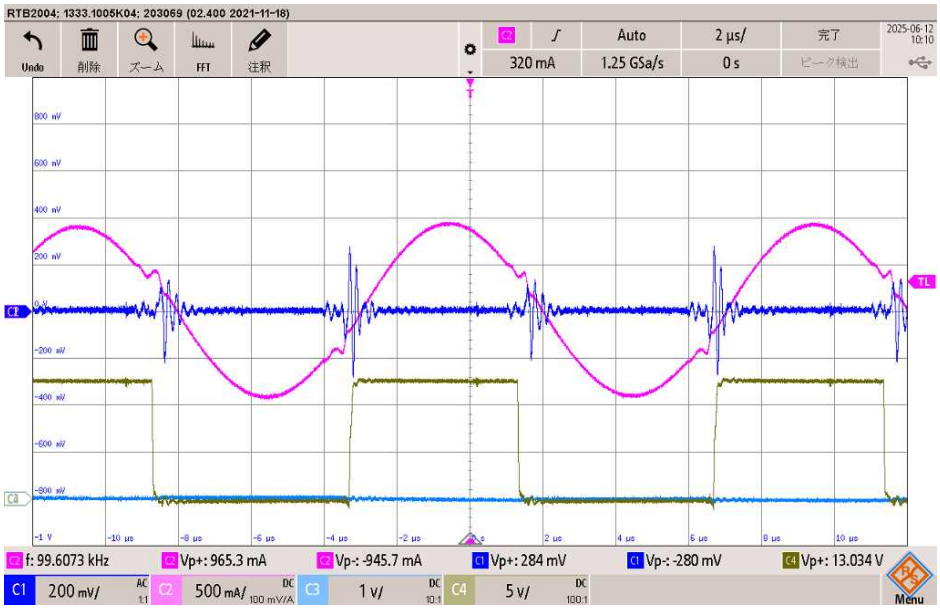
Input: DC380V (PFC output), Output 1: 5V 10A (at rated load), Output 2: 24V 2A (at rated load)

(However, the 5V output voltage is set to the lower limit voltage of 4.7V.)

1-1-1. Steady-state waveform 1

Measure the T1 primary current waveform, TR5 gate voltage, and 5V output voltage at 100% rated load.

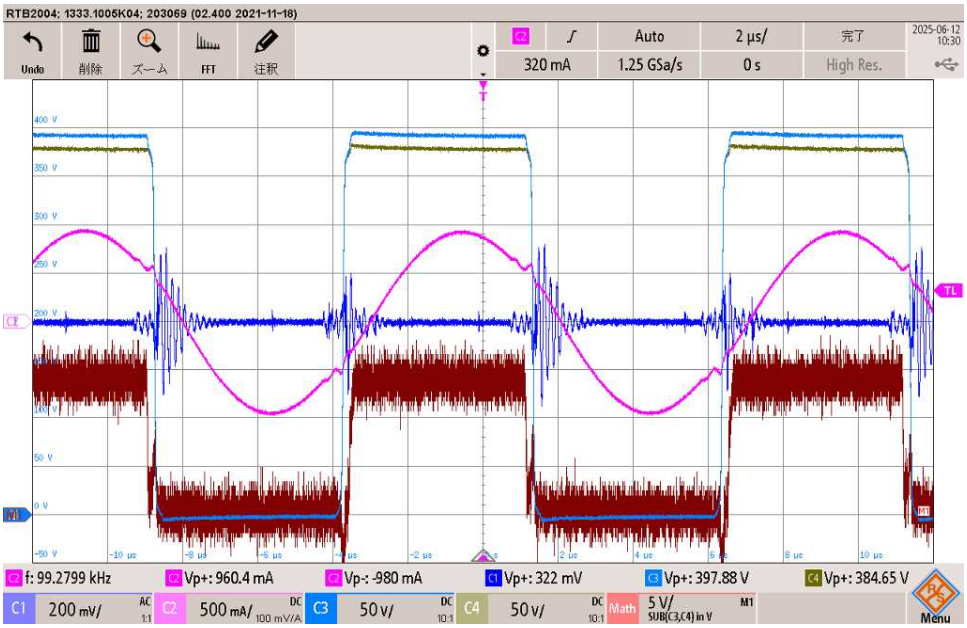
H: [2 μ sec/div]



1-1-2. Steady-state waveform 2

Measure the T1 primary current waveform, TR3 gate voltage, and 5V output voltage at 100% rated load.

The TR3 gate voltage is measured by calculating the difference between the CH3 (TR3-G-GND) and CH4 (TR3-S-GND) waveforms instead of using a differential probe.



1-2. TR3, TR5 gate voltage waveforms when the load suddenly changes

<Measurement conditions>

Input: DC380V (PFC output)

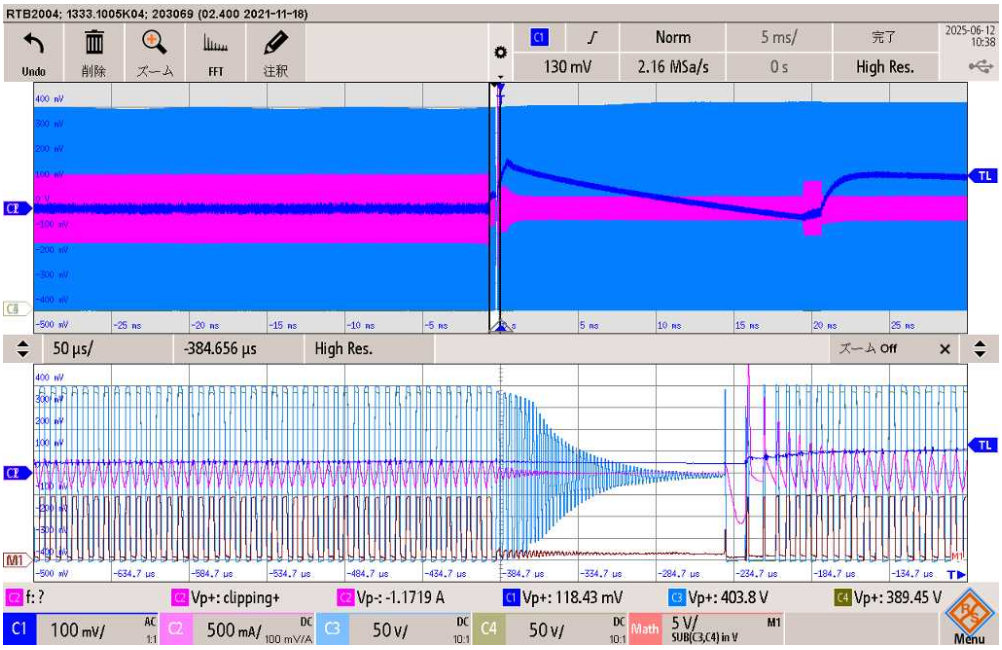
Output 1: 5V 10A (no-load set voltage: 4.7V, load current: 100% to 0% sudden change)

Output 2: 24V 2A (no load)

1-2-1.Measurement of gate voltage of TR3

Waveform when 5V output suddenly changes from 100% to 0% [5ms/div], Enlarged waveform 1 [50 μ sec/div]　The gate waveform of TR3 stops for a certain period when the 5V output suddenly changes from 100% to 0%. (See Enlarged waveform 1)

Could this be the reason why the 5V output rises to about 200mV when the transient change is 0%?

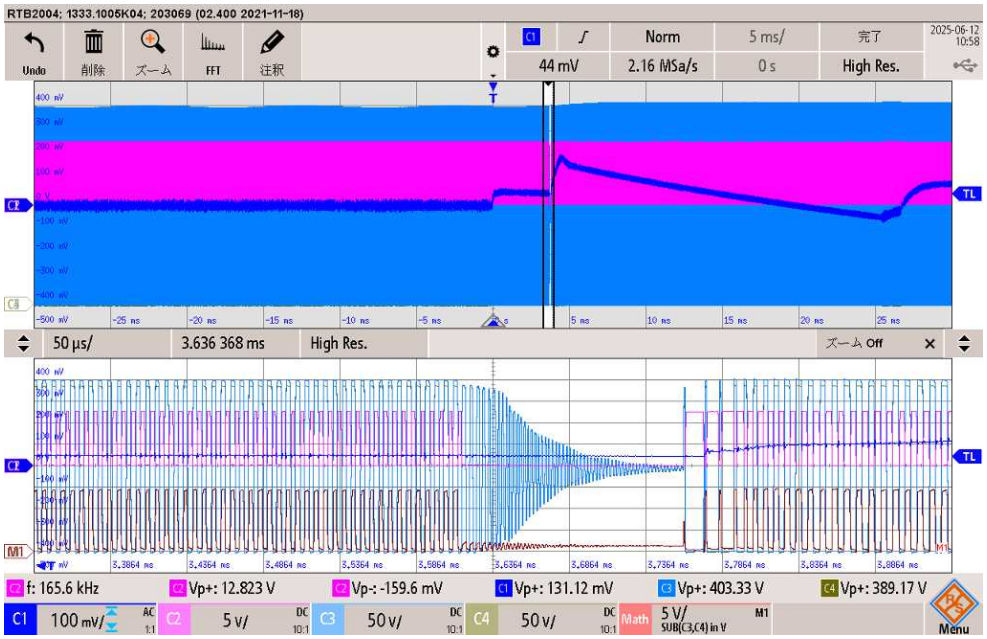


C1:5Vout[100mV/div], C2:T1 primary current[500mA/div], C3:TR3-gate voltage[50V/div], C4:TR3-source voltage[50V/div], Math:TR3g-s voltage[5V/div]

1-2-2. Measurement of gate voltage of TR3 and TR4 1

Waveform when 5V output suddenly changes from 100% to 0% [5ms/div], Enlarged waveform 2 [50 μ sec/div]

Instead of T1 primary current, TR5-gate voltage was measured, and it was confirmed that the gate voltage of both TR3 and TR5 stopped for a certain period (about 150 μ sec) when the 5V output suddenly changed from 100% to 0%.

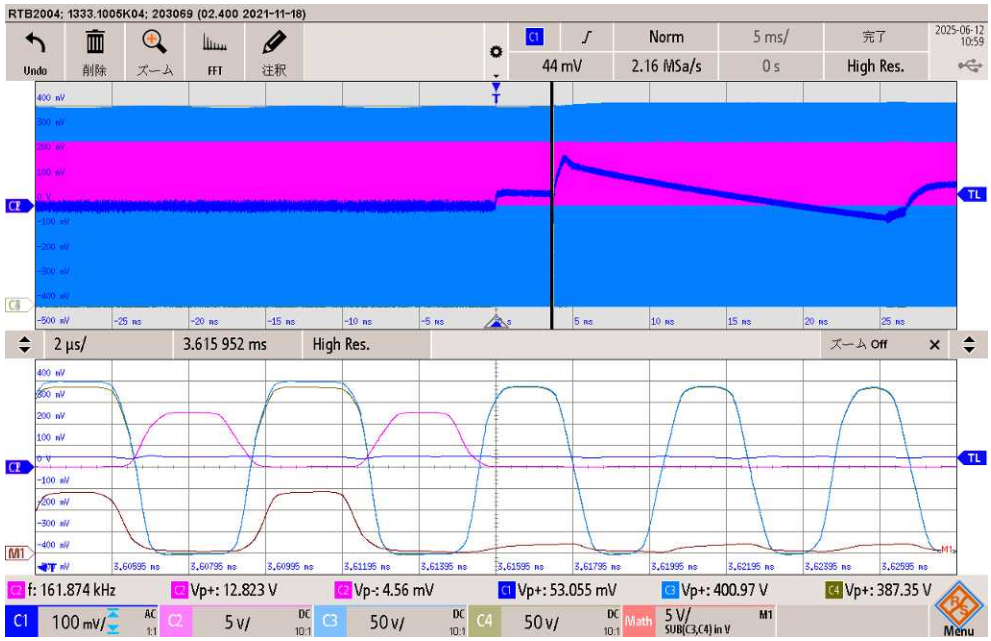


C1:5Vout[100mV/div], C2:TR5g-s voltage[5V/div], C3:TR3-gate voltage[50V/div], C4:TR3-source voltage[50V/div], Math:TR3g-s voltage[5V/div]

1-2-3. Measurement of gate voltage of TR3 and TR4 2

Waveform when 5V output suddenly changes from 100% to 0% [5ms/div], Enlarged waveform 3 [2 μ sec/div]

Enlarged waveform of gate voltage of TR3 and TR5 at the moment when 5V output suddenly changes from 100% to 0%.



2. Answer to Question 2

The designed crossover frequency (fT) and phase margin (θ) are as follows.

Crossover frequency (fT): 5k to 10kHz

Phase margin (θ): 60° to 70°

3. Answer to question 3

The ESR of the 5V output capacitors (C80, C81, C85) is 15mΩ (max) at 20°C_100kHz.

End