UCC28019A: Changes from UCC28019

Original UCC28019	New UCC28019A
• Has 2V step on internal VCOMP during EDR and SS (VSENSE < 4.75V) – Sudden increase in current loop gain which resulted in audible noise during transients and start up	• 2V step removed – No step during EDR results in no audible noise during transients – But the control loop requires approximately 2V offset before SS begins to minimize the delay at start up •A pre-start current charges external C_{VCOMP} to 1.9V **ONLY** before SS to decrease start time and initiate the increase in duty cycle
• Voltage error amp has 120uA slew rate correction current during EDR – This sudden step change in the current amplifier would result in brief input current distortion and audible noise	• Voltage error amp transconductance is increased to 440uS during EDR – Sudden step change replaced with a continuous gain change results in the input current much less distorted and no audible noise during transients
• SS ends when VSENSE = 4.75V (95% of nominal) – Usually, EDR activated (VSENSE = 4.75V) – Noise from boost inductor may result	• SS ends when VSENSE = 4.95V (99% of nominal) – Avoids activating EDR with V_{OUT} ripple voltage – With no EDR immediately after SS, there should be no noise from inductor at start up
• No open-circuit protection on ISENSE – If ISENSE pin open-circuit, the result is the same as if ISENSE were shorted to GND: maximum duty cycle => OVP => erratic current spikes on input	• Open-circuit protection added to ISENSE – ISENSE pin has small pull up current (~1.5uA) to trigger a fault condition and shut down the IC if pin is open-circuit
• OVP condition disables the GATE output when VSENSE exceeds 105% of the reference voltage – Resulting in inductor noise due to the chopped AC current when GATE disabled then turned on during start up into light load conditions	• Unchanged in UCC28019A – Slow loop response may result in converter hitting OVP when turned on into light load conditions